DAQ

DAQPad™-6020E
User Manual

Multifunction I/O Devices for USB

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About This Manual

This manual describes the electrical and mechanical aspects of the DAQPad-6020E and contains information concerning its operation and programming. The DAQPad-6020E is a high-performance multifunction analog, digital, and timing I/O device for USB compatible computers.

Organization of This Manual

The *DAQPad-6020E User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the DAQPad-6020E, lists what you need to get started, explains how to unpack your DAQPad-6020E, and describes the optional software and optional equipment.
- Chapter 2, *Installation and Configuration*, explains how to install and configure your DAQPad-6020E.
- Chapter 3, *Hardware Overview*, presents an overview of the hardware functions on your DAQPad-6020E.
- Chapter 4, *Signal Connections*, describes how to make input and output signal connections to your DAQPad-6020E via the device I/O connector.
- Chapter 5, *Calibration*, discusses the calibration procedures for your DAQPad-6020E.
- Appendix A, *Specifications*, lists the specifications of the DAQPad-6020E.
- Appendix B, *Optional Cable Connector Descriptions*, describes the connectors on the optional cables for the DAQPad-6020E.
- Appendix C, *Measuring More than Eight Channels with the DAQPad-6020E (BNC)*, explains how to measure more than eight channels with the DAQPad-6020E (BNC). If you are measuring eight channels or less, you do not need to read this section.
- Appendix D, *Common Questions*, contains a list of commonly asked questions and their answers relating to usage and special features of your DAQPad-6020E.
- Appendix E, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.

- The *Glossary* contains an alphabetical list and description of terms used in this manual, including acronyms, abbreviations, metric prefixes, mnemonics, and symbols.
- The *Index* alphabetically lists topics covered in this manual, including the page where you can find the topic.

Conventions Used in This Manual

The following conventions are used in this manual.

<>	Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, ACH<0..15>.
♦	The ♦ symbol indicates that the text following it applies only to a specific DAQPad-6020E device.
☞	This icon to the left of bold italicized text denotes a note, which alerts you to important information.
⚠	This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
bold	Bold text denotes the names of menus, menu items, parameters, dialog boxes, dialog box buttons or options, icons, windows, Windows 95 tabs, or LEDs.
bold italic	Bold italic text denotes an activity objective, note, caution, or warning.
DAQPad-6020E	This term refers to either or both of the two models with 68-pin I/O connectors. One of these models is half-size; the other is full size.
DAQPad-6020E (BNC)	This term refers only to the DAQPad-6020E with BNC connectors on the front panel.
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text from which you supply the appropriate word or value, as in Windows 3.*x*.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
PC	PC refers to your personal computer.

SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ devices.

National Instruments Documentation

The *DAQPad-6020E User Manual* is one piece of the documentation set for your DAQ system. You could have any of several types of manuals depending on the hardware and software in your system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW and LabWindows/CVI documentation sets and the NI-DAQ documentation. After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- *SCXI Chassis Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and installation instructions.

Related Documentation

The following National Instruments document contains information you may find helpful: Application Note 025, *Field Wiring and Noise Considerations for Analog Signals*

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix E, *Customer Communication*, at the end of this manual.

1

Introduction

This chapter describes the DAQPad-6020E, lists what you need to get started, explains how to unpack your DAQPad-6020E, and describes the optional software and optional equipment.

About the DAQPad-6020E

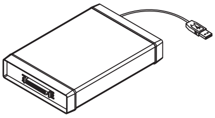
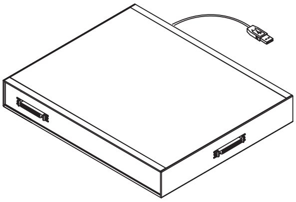
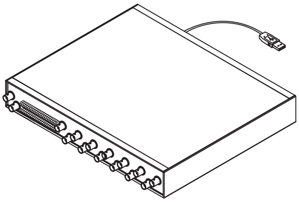
Thank you for buying a National Instruments DAQPad-6020E. The DAQPad-6020E is a USB-compatible multifunction analog, digital, and timing I/O device for USB-compatible computers. This product features a 12-bit ADC with eight differential/16 single-ended inputs, two 12-bit DACs with voltage outputs, eight lines of TTL-compatible digital I/O, and two 24-bit counter/timers for timing I/O. The DAQPad-6020E has no DIP switches, jumpers, or potentiometers and is easily configured and calibrated using software.

The DAQPad-6020E uses the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns.

The DAQPad-6020E is a USB data acquisition (DAQ) device. USB compatibility supports Plug and Play and also hot or powered insertion into the USB, so you do not need to power down your computer to connect the DAQPad.

There are three versions of the DAQPad-6020E offering different I/O connectivity and form factors. These versions are illustrated in Table 1-1.

Table 1-1. DAQPad-6020E Models

DAQ Device	I/O Connector	Form Factor	
DAQPad-6020E	68-pin SCSI II Male	Half-size box (5.8 in x 8.4 in x 1.5 in) Desktop use	
DAQPad-6020E	68-pin SCSI II Male	Full-size box (12.1 in x 10 in x 1.7 in) Rack-mountable, stackable	
DAQPad-6020E (BNC)	BNC and removable screw terminals	Full-size box (12.1 in x 10 in x 1.7 in) Rack-mountable, stackable	

The DAQPad-6020E can connect to an SCXI system (68-pin I/O connector versions only) so that you can acquire over 3,000 analog signals from thermocouples, RTDs, strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control. SCXI is the instrumentation front end for plug-in DAQ devices.

Detailed specifications of the DAQPad-6020E are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your DAQPad-6020E, you will need the following:

- ☐ DAQPad-6020E device
- ☐ *DAQPad-6020E User Manual*
- ☐ One of the following software packages and documentation
    - – NI-DAQ for PC compatibles
    - – LabVIEW
    - – LabWindows/CVI
    - – ComponentWorks
    - – VirtualBench
- ☐ Your computer

Unpacking

Your DAQPad-6020E is shipped in a fully shielded case, and no electrostatic precautions are necessary. However, for your own safety and to protect your DAQPad device, *never* attempt to touch the connector pins.

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ hardware. You can use LabVIEW, LabWindows/CVI, ComponentWorks, VirtualBench, or NI-DAQ.

National Instruments Application Software

LabVIEW features interactive graphics, a state-of-the art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics and a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using

National Instruments DAQ hardware, is included with LabWindows/CVI. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

ComponentWorks contains tools for data acquisition and instrument control built on NI-DAQ driver software. ComponentWorks provides a higher-level programming interface for building virtual instruments through standard OLE controls and DLLs. With ComponentWorks, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using LabVIEW, LabWindows/CVI, ComponentWorks, or VirtualBench software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, Real-Time System Integration (RTSI), calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples for high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance, even simultaneously.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages or NI-DAQ software, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

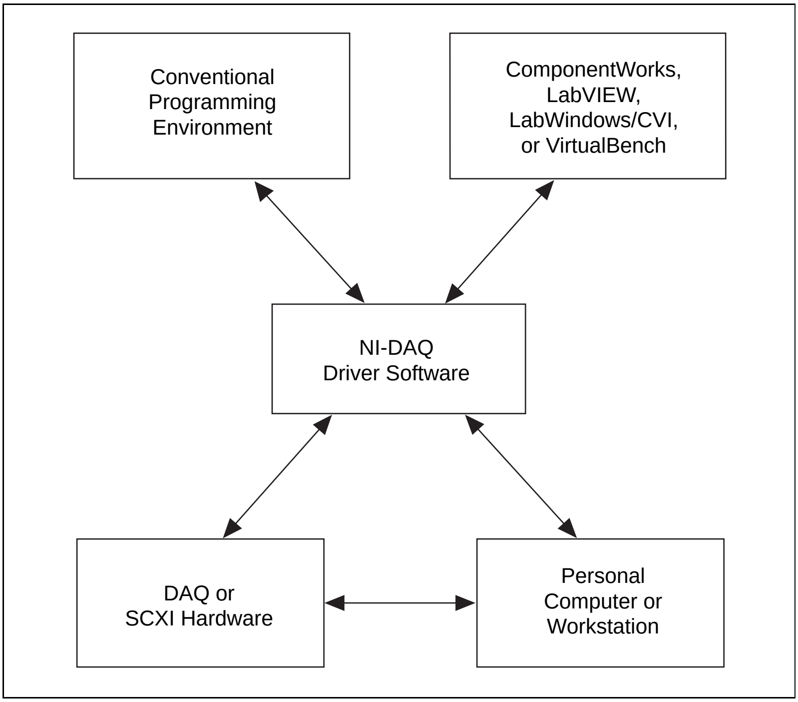


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

You can use your DAQPad-6020E, together with other DAQPad, PC, AT, DAQCard, and other DAQ and SCXI hardware, with the NI-DAQ software for PC compatibles.

Optional Equipment

National Instruments offers a variety of products to use with your DAQPad-6020E, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50 and 68-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3072 channels.
- Low channel count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

The following list gives recommended part numbers for connectors that mate to the I/O connector on your DAQPad-6020E:

- Mating connectors and a backshell kit for making custom 68-pin cables are available from National Instruments (part number 776832-01)
- Honda 68-position, solder cup, female connector (part number PCS-E68FS)
- Honda backshell (part number PCS-E68LKPA)

2

Installation and Configuration

This chapter explains how to install and configure your DAQPad-6020E.

Software Installation

You should install your software before you install your DAQPad-6020E. If you are using LabVIEW, LabWindows/CVI, ComponentWorks, or VirtualBench application software, install this software before installing NI-DAQ driver software. Refer to your software release notes for installation instructions.

☞ **Note** ***The DAQPad-6020E requires NI-DAQ 6.5 or later. To ensure that you have the latest version of NI-DAQ, install it from the CD that ships with your device.***

To install NI-DAQ, refer to your NI-DAQ release notes. Find the installation section for your operating system and follow the instructions given there.

Hardware Installation

You can attach your DAQPad-6020E to any available USB port.

The following are general installation instructions, but consult your personal computer user manual or technical reference manual for specific instructions and warnings.

☞ **Note** ***The DAQPad-6020E requires NI-DAQ 6.5 or later. To ensure proper operation of your DAQPad device, follow the instructions in the sequence shown below. Otherwise, your DAQPad might not initialize properly, and you will need to turn off the DAQPad rocker switch and restart your DAQPad device.***

☞ **Note** ***If you are using the BP-1 battery pack, follow the installation instructions in your BP-1 installation guide and disregard steps 1 and 3 in this manual. If you are NOT using the BP-1 battery pack, follow the instructions below.***

1. Verify that the voltage on the external power supply matches the voltage (120 or 230 VAC) supplied in your area.

2. Verify that the external power supply voltage matches the power supply required by the DAQPad-6020E. You can find the supply voltage information on the external power supply and also on the rear panel of the DAQPad-6020E.
3. Connect one end of the external supply to the electrical outlet. Connect the other end to the rear panel jack. Notice that the jack has a locking plug. You might need this lock if the connection between the external power supply and the DAQPad-6020E does not seem secure.
4. Connect the USB cable from the computer port or from any other hub to the port on the DAQPad-6020E.

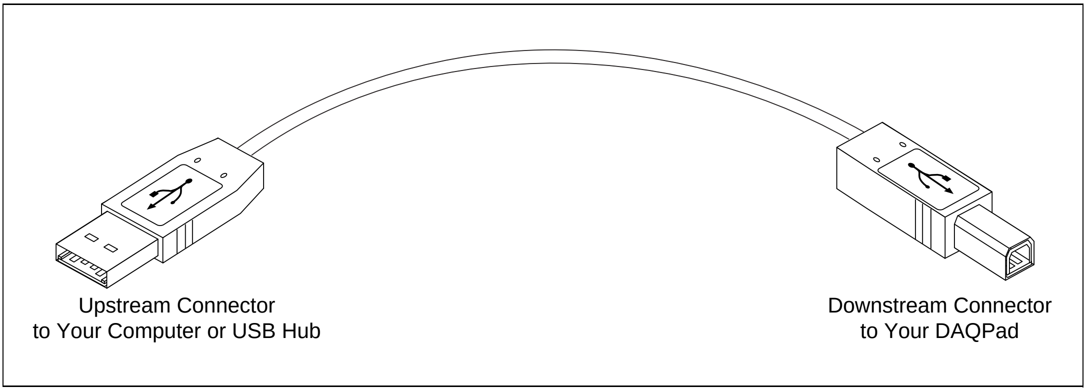


Figure 2-1. Cable between Your Computer or USB Hub and Your DAQPad Device

5. Flip the rocker switch to turn on the power for the DAQPad-6020E. Your computer should detect the DAQPad device immediately, and when the computer recognizes the DAQPad device, the LED on the front panel blinks or lights up, depending on the status of your device.
6. If the LED comes on after the DAQPad is powered and connected to the host, it is functioning properly. Refer to Table 2-1 for LED pattern descriptions.
7. Configure your DAQPad device and any accessories with the NI-DAQ Configuration Utility.

Table 2-1. LED Patterns for DAQPad-6020E States

LED	DAQPad-6020E State	Description
On	Configured state	Your DAQPad device is configured.
Off	Off or in the low-power, suspend mode	The DAQPad device turns off or goes into the low-power, suspend mode when the computer is powered down.
1 blink	Attached state	Your DAQPad is recognized but not configured.
2 blinks	Addressed state	This pattern is displayed if the host computer detects your DAQPad device but cannot configure it because NI-DAQ is not properly installed, or there are no system resources available. Check your software installation.
4 blinks	General error state	If this pattern is displayed, contact National Instruments.

When the LED blinks, it turns on and off in one second intervals for as many times as necessary, then waits three seconds before repeating the cycle.

Configuration

The DAQPad-6020E is a completely software-configurable, hot Plug and Play device. Plug and Play services query the device and allocate the required resources. The operating system enables the device for operation. Refer to your software documentation for more information.

Power Considerations

The DAQPad-6020E will be powered if the rocker switch is on and the external power supply is connected, whether or not the USB cable is attached. If you are using a battery pack to power the DAQPad-6020E or if power conseravation is an issue, either disconnect the power cord or throw the rocker switch on the rear panel to turn off the DAQPad-6020E.

3

Hardware Overview

This chapter presents an overview of the hardware functions on your DAQPad-6020E.

Figure 3-1 shows the block diagram for the DAQPad-6020E.

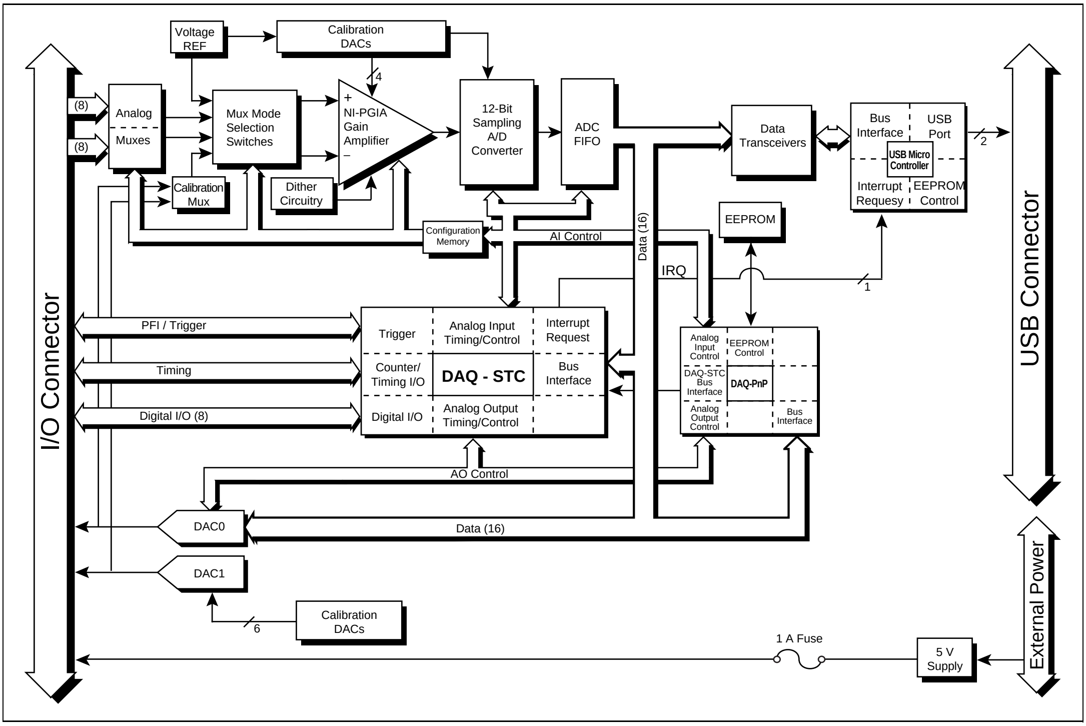


Figure 3-1. DAQPad-6020E Block Diagram

Analog Input

The analog input section of the DAQPad-6020E is software configurable. You can select different analog input configurations through application software designed to control the DAQPad-6020E. The following sections describe in detail each of the analog input categories.

Input Mode

The DAQPad-6020E has three different input modes—nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configuration uses up to 16 channels. The DIFF input configuration uses up to eight channels. Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially configured channels and eight single-ended channels. Table 3-1 describes the three input configurations.

☞ **Note** ***On the DAQPad-6020E (BNC), there are eight analog input BNC connectors to provide easy connectivity to eight differential channels in DIFF mode.***

Table 3-1. DAQPad-6020E Input Configurations

Configuration	Description
DIFF	A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to the analog input ground (AIGND) signal.
NRSE	A channel configured in NRSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the analog input sense (AISENSE) signal.

For more information about the three types of input configuration, refer to Chapter 4, *Signal Connections*.

Input Polarity and Input Range

The DAQPad-6020E has two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. The DAQPad-6020E has a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V). You can program polarity and range settings on a per channel basis so that you can configure each input channel uniquely.

The software-programmable gain on these devices increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. The DAQPad-6020E has gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and is suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Precision[1]
0 to +10 V	1.0	0 to +10 V	2.44 mV
	2.0	0 to +5 V	1.22 mV
	5.0	0 to +2 V	488.28 µV
	0.0	0 to +1 V	244.14 µV
	0.0	0 to +500 mV	122.07 µV
	50.0	0 to +200 mV	48.83 µV
	100.0	0 to +100 mV	24.41 µV
–5 to +5 V	0.5	–10 to +10 V	4.88 mV
	1.0	–5 to +5 V	2.44 mV
	2.0	–2.5 to +2.5 V	1.22 mV
	5.0	–1 to +1 V	488.28 µV
	10.0	–500 to +500 mV	244.14 µV
	20.0	–250 to +250 mV	122.07 µV
	50.0	–100 to +100 mV	48.83 µV
	100.0	–50 to +50 mV	24.41 µV

[1] The value of 1 LSB of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

See Appendix A, *Specifications*, for absolute maximum ratings.

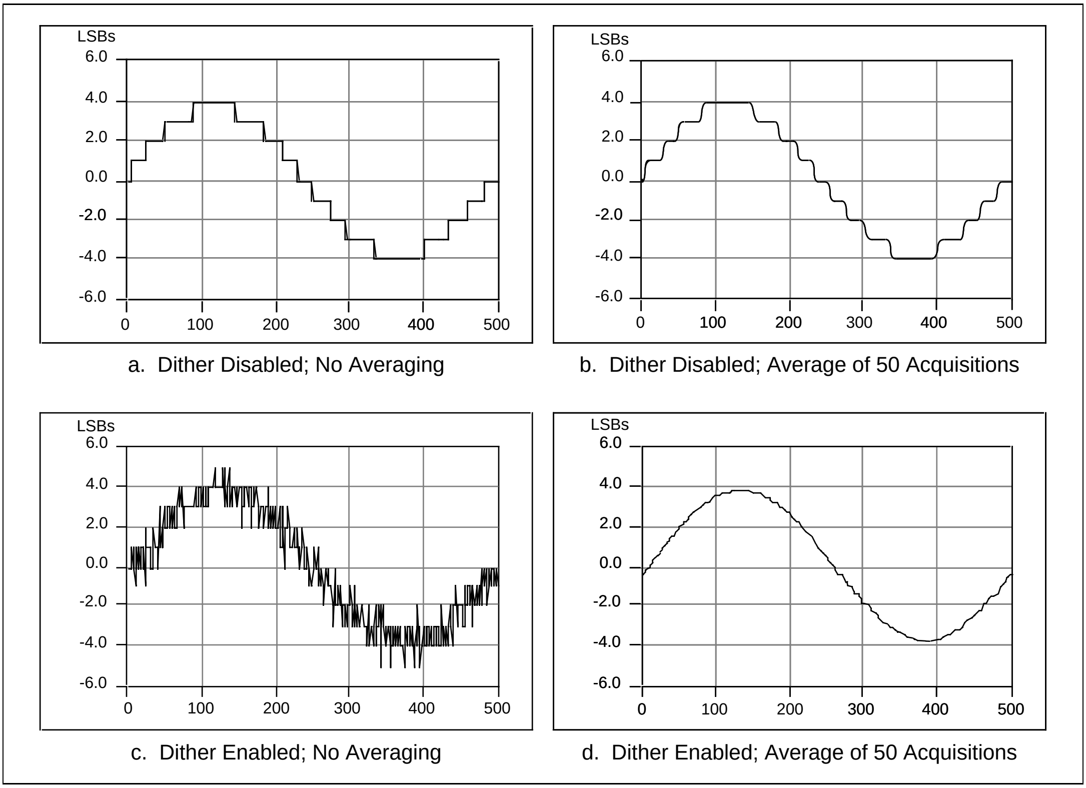
Considerations for Selecting Input Ranges

The input polarity and range that you select depend on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but can result in the input signal going out of range. For best results, you should match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal will not be negative (below 0 V), unipolar input polarity is best. However, if the signal is negative or equal to zero, inaccurate readings occur when you use unipolar input polarity.

Dither

When you enable dither, you add approximately 0.5 LSB rms of white Gaussian noise to the signal to be converted by the ADC. You can use this addition for applications that involve averaging to increase the resolution of your DAQPad-6020E, as in calibration or spectral analysis. In such applications, noise modulation is decreased and differential linearity is improved by the addition of the dither. When taking DC measurements, such as when checking the device calibration, you should enable dither and average about 1,000 points to take a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution. For high-speed applications not involving averaging or spectral analysis, you can disable the dither to reduce noise. You enable and disable the dither circuitry through software.

Figure 3-2 illustrates the effect of dither on signal acquisition. Figure 3-2a shows a small (±4 LSB) sine wave acquired with dither off. The quantization of the ADC is clearly visible. Figure 3-2b shows what happens when 50 such acquisitions are averaged together; quantization is still plainly visible. In Figure 3-2c, the sine wave is acquired with dither on. A considerable amount of noise is visible. But averaging about 50 such acquisitions, as shown in Figure 3-2d, eliminates both the added noise and the effects of quantization. Dither has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.



a. Dither Disabled; No Averaging

b. Dither Disabled; Average of 50 Acquisitions

c. Dither Enabled; No Averaging

d. Dither Enabled; Average of 50 Acquisitions

Figure 3-2. The Effects of Dither

Multiple-Channel Scanning Considerations

The DAQPad-6020E can scan multiple channels at a very high rate; however, you should pay careful attention when you scan multiple channels, because switching gains can extend the settling time for each of your devices. The settling time for the DAQPad-6020E is independent of the selected gain, even at the maximum sampling rate. The settling time for the high channel count and very high-speed devices is dependent on the number of gains used, which can affect the useful sampling rate for a given gain. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times for the DAQPad-6020E.

When the DAQPad-6020E is scanning among channels at various gains, the settling times may increase. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range.

For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode).

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 12-bit device to settle within 0.012% (120 ppm or 1/2 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle to within 0.0003% (3 ppm or 1/80 LSB) of the 4 V step. It may take as long as 100 µs for the circuitry to settle this much. For a 16-bit device to settle within 0.0015% (15 ppm or 1 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle within 0.00004% (0.4 ppm or 1/400 LSB) of the 4 V step. It can take as long as 200 µs for the circuitry to settle this much. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times also can increase when scanning high-impedance signals due to a phenomenon called *charge injection*, where the analog input multiplexer injects a small amount of charge into each signal source when that source is selected. If the source impedance is not low enough, the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, you should keep source impedances under 1 kΩ to perform high-speed scanning.

Due to the previously described limitations of settling times resulting from these conditions, multiple-channel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

Analog Output

The DAQPad-6020E supplies two channels of analog output voltage at the I/O connector. You can select the reference and range for the analog output circuitry through software. The reference can be either internal or external, whereas the range can be either bipolar or unipolar.

Analog Output Reference Selection

You can connect each D/A converter (DAC) to the DAQPad-6020E internal reference of 10 V or to the external reference signal connected to the external reference (EXTREF) pin on the I/O connector. This signal applied to EXTREF should be between –11 and +11V. You do not need to configure both channels for the same mode.

Analog Output Polarity Selection

You can configure each analog output channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the analog output. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the analog output. V_{ref} is the voltage reference used by the DACs in the analog output circuitry and can be either the +10 V onboard reference or an externally supplied reference between –11 and +11 V. You do not need to configure both channels for the same range.

Selecting a bipolar range for a particular DAC means that any data written to that DAC will be interpreted as two's complement format. In two's complement mode, data values written to the analog output channel can be either positive or negative. If you select unipolar range, data is interpreted in straight binary format. In straight binary mode, data values written to the analog output channel range must be positive.

Digital I/O

The DAQPad-6020E contains eight lines of digital I/O for general-purpose use. You can configure each line individually through software for either input or output. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a very flexible interface for connecting timing signals to other devices or external circuitry. Your DAQPad-6020E uses Programmable Function Input (PFI) pins on the I/O connector for connecting to external circuitry. These connections are designed to enable the DAQPad-6020E both to control and be controlled by other devices and circuits.

A total of 13 timing signals internal to the DAQ-STC can be controlled by an external source. These timing signals also can be controlled by signals generated internally to the DAQ-STC. These selections are fully software configurable. The signal routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-3.

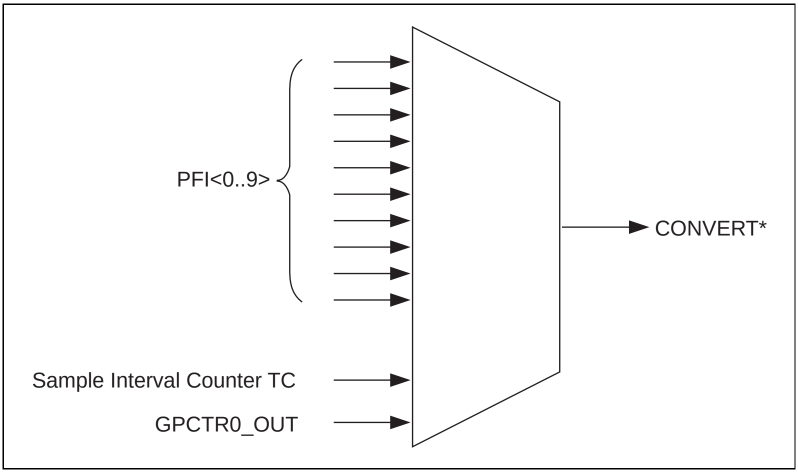


Figure 3-3. CONVERT* Signal Routing

This figure shows that the CONVERT* signal can be generated from a number of sources, including the external signals PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFIs as the external source for a given timing signal. Keep in mind that any of the PFIs can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications.

You also can enable each of the PFI pins individually to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

4

Signal Connections

This chapter describes how to make input and output signal connections to your DAQPad-6020E via the device I/O connector.

- DAQPad-6020E
  The I/O connector for the DAQPad-6020E has 68 pins that you can connect to 68-pin accessories with the SH6868 shielded cable or the R6868 ribbon cable. You can connect your device to 50-pin signal conditioning modules and terminal blocks using the SH6850 shielded cable or R6850 ribbon cable.

- DAQPad-6020E (BNC)
  The BNC version allows connection to all analog and some digital signals via BNC connectors. The remaining digital signals can be accessed via the removable screw terminal block on the front panel of the DAQPad-6020E (BNC).

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the DAQPad-6020E. Refer to Appendix B, *Optional Cable Connector Descriptions*, for the pin assignments for the 50-pin connectors. A signal description follows the connector pinouts.

Figure 4-2 shows the pin assignment for the I/O connector on the DAQPad-6020E (BNC).

Warning ***Connections that exceed any of the maximum ratings of input or output signals on the DAQPad-6020E can damage the DAQPad-6020E and the PC. Maximum input ratings for each signal are given in Table 4-1 in the*** *Protection* ***column. National Instruments is NOT liable for any damages resulting from such signal connections.***

Tip ***Always ground any unused analog input channels. Floating (unconnected) input channels can degrade measurements.***

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT	22	56	AIGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

Figure 4-1. I/O Connector Pin Assignment for the DAQPad-6020E 68-Pin I/O Connector

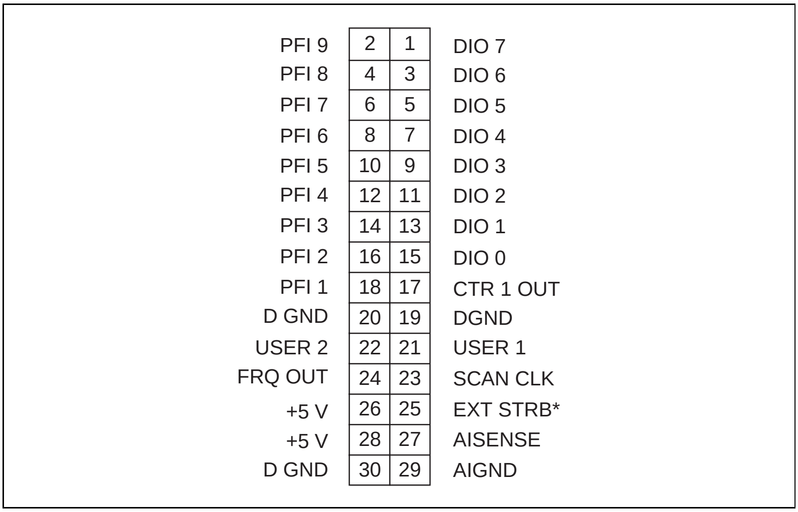


Figure 4-2. I/O Connector Pin Assignment for the DAQPad-6020E (BNC).

I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on your DAQPad-6020E.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.
EXTREF	AOGND	Input	External Reference—This is the external reference input for the analog output circuitry.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on your DAQPad-6020E.

Signal Name	Reference	Direction	Description (Continued)
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your DAQPad-6020E.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is either one of the Programmable Function Inputs (PFIs) or the source for the hardware analog trigger. PFI signals are explained in the *Timing Connections* section later in this chapter.
		Output	As an output, this is the TRIG1 signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is one of the PFIs.
		Output	As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is one of the PFIs.
		Output	As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.

Signal Name	**Reference**	**Direction**	**Description (Continued)**
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is one of the PFIs.
		Output	As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is one of the PFIs.
		Output	As an output, this is the STARTSCAN signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-1 shows the I/O signal summary for the DAQPad-6020E.

Table 4-1. I/O Signal Summary

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 50 pF	35/25	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 50 pF	35/25	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	15 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	15 V/µs	—
EXTREF	AI	10 kΩ	35/25	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu[1]
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-1. I/O Signal Summary (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc-}0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

[1] DIO <6..7> are also pulled down with a 50 kΩ resistor.

AI = Analog Input DIO = Digital Input/Output pu = pullup
AO = Analog Output DO = Digital Output

Note: ***The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.***

Analog Input Signal Connections

The analog input signals are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are tied to the 16 analog input channels of your DAQPad-6020E. In single-ended mode, signals connected to ACH<0..15> are routed to the positive input of the device PGIA. In differential mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

⚠ **Caution** ***Exceeding the differential and common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage the DAQPad-6020E and the PC. National Instruments is NOT liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in Table 4-1 in the*** *Protection* ***column.***

In NRSE mode, the AISENSE signals are connected internally to the negative input of the DAQPad-6020E PGIA when their corresponding channels are selected. In DIFF and RSE modes, these signals are left unconnected.

AIGND is an analog input common signal that is routed directly to the ground tie point on the DAQPad-6020E. You can use this signal for a general analog ground tie point to your DAQPad-6020E if necessary.

Connection of analog input signals to your DAQPad-6020E depends on the configuration of the analog input channels you are using and the type of input signal source. With the different configurations, you can use the PGIA in different ways. Figure 4-3 shows a diagram of your DAQPad-6020E PGIA.

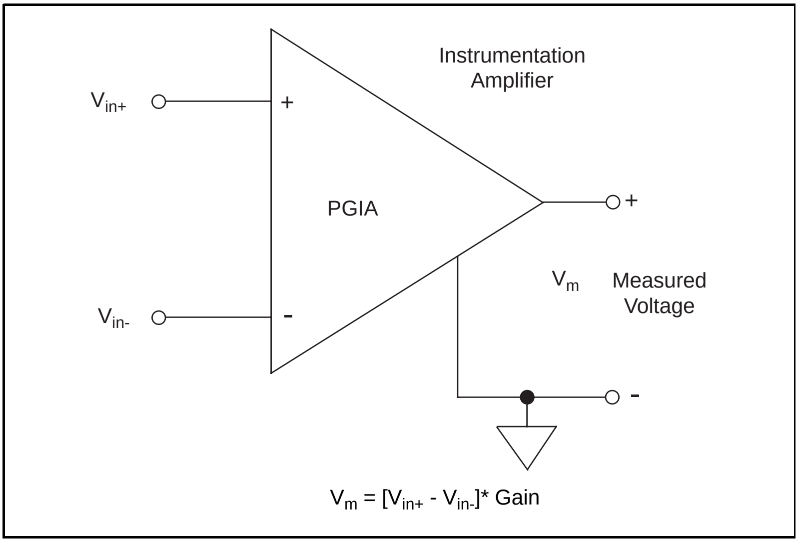


Figure 4-3. DAQPad-6020E PGIA

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to your DAQPad-6020E. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the device. Your DAQPad-6020E A/D converter (ADC) measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the device. If you have a floating source (FS), you should reference the signal to ground by using the RSE input mode or the DIFF input configuration with bias resistors (see the *Differential Connections for Nonreferenced or Floating Signal Sources* section later in this chapter). If you have a grounded source (GS), you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

☞ **Note** ***The DAQPad-6020E (BNC) contains built-in user switchable ground referencing resistors as shown in Figure 4-3. The factory default configuration is ground referencing resistor engaged, that is, source type switches S0 through S7 are closed (FS position). This configuration is useful in measuring floating signal sources.***

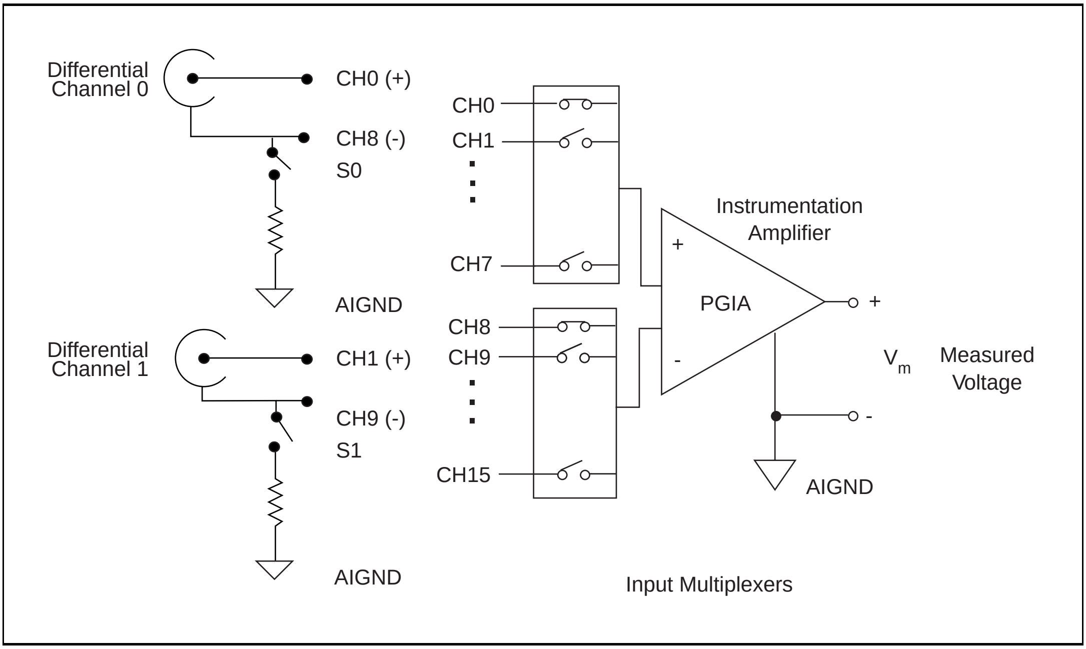


Figure 4-4. DAQPad-6020E (BNC) Analog Input Signals Path DIFF Input Mode

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is one that is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to your DAQPad-6020E analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

On the DAQPad-6020E (BNC), flip the source type switch (S0 through S7) to the FS position to measure floating signal sources.

Ground-Referenced Signal Sources

A ground-referenced signal source is one that is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the DAQPad-6020E, assuming that the PC is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

On the DAQPad-6020E (BNC), ensure that the source type switches (S0 through S7) are in the GS position to measure ground-referenced signal sources.

Input Configurations

You can configure your DAQPad-6020E for one of three input modes—NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Figure 4-5 summarizes the recommended input configuration for both types of signal sources.

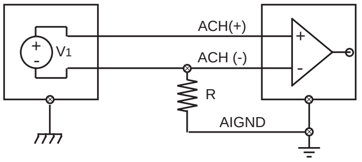
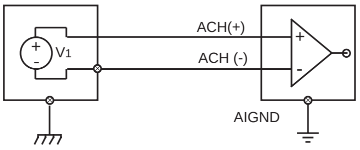
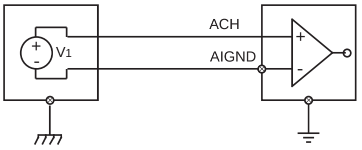
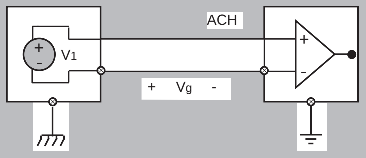
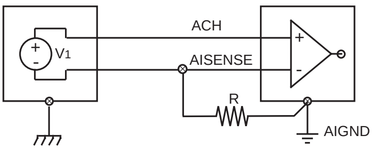
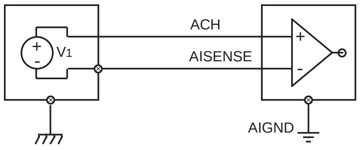
Input	**Signal Source Type**	
	Floating Signal Source (Not Connected to Building Ground)	**Grounded Signal Source**
	Examples • Ungrounded Thermocouples • Signal conditioning with isolated outputs • Battery devices	Examples • Plug-in instruments with nonisolated outputs
Differential (DIFF)	 See text for information on bias resistors.	
Single-Ended — Ground Referenced (RSE)		NOT RECOMMENDED  Ground-loop losses, V_g, are added to measured signal
Single-Ended — Nonreferenced (NRSE)	 See text for information on bias resistors.	

Figure 4-5. Summary of Analog Input Connections on the DAQPad-6020E (68-pin I/O Connector)

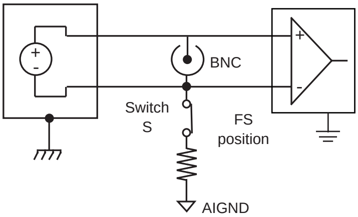
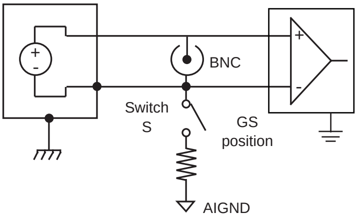
Input Mode	**Signal Source Type**	
	Floating Signal Source (Not Connected to Building Ground)	**Grounded Signal Source**
	Examples • Signal conditioning with isolated outputs • Battery devices	Examples • Plug-in instruments with nonisolated outputs
Differential Recommended		

Figure 4-6. Summary of Analog Input Connections DAQPad-6020E (BNC)

If your application requires measuring more than eight channel, please refer to Appendix C, Measuring More than Eight Channels with the DAQPad-6020E (BNC).

Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the DAQPad-6020E analog input signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight analog input channels are available.

You should use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).

- The leads connecting the signal to the DAQPad-6020E are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked-up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-7 shows how to connect a ground-referenced signal source to a DAQPad-6020E channel configured in DIFF input mode.

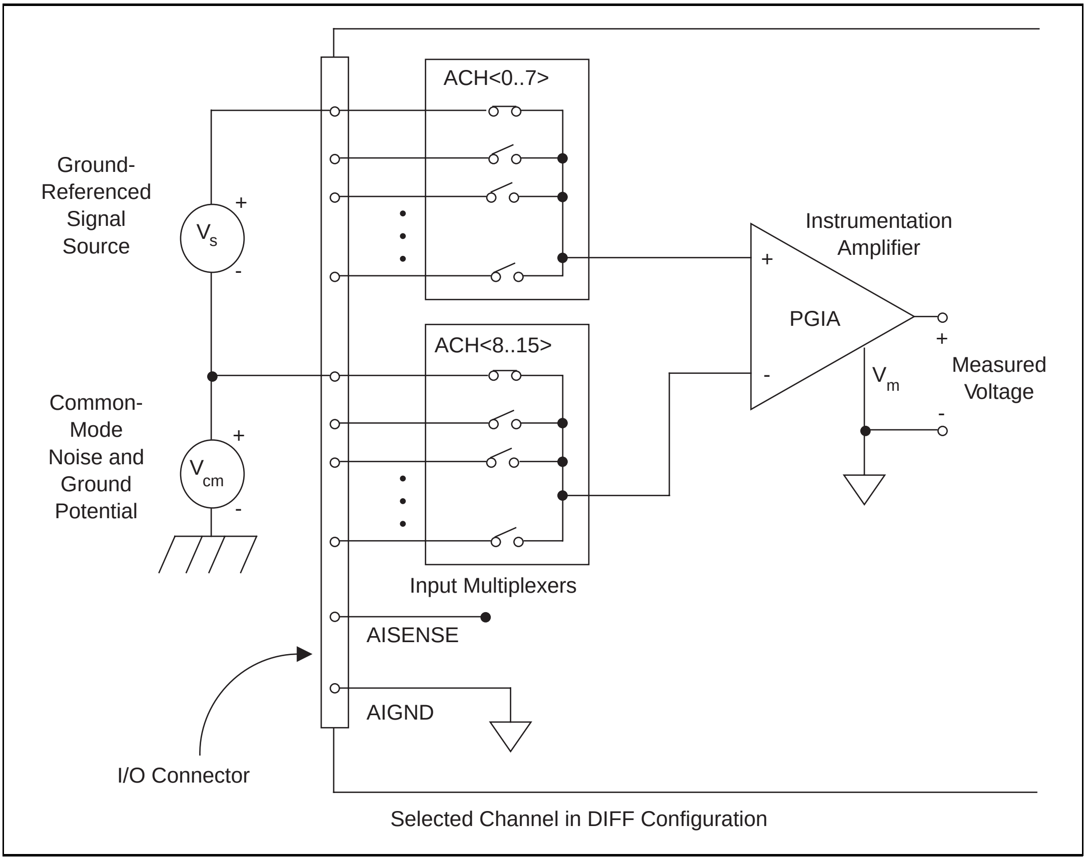


Figure 4-7. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the DAQPad-6020E ground, shown as V_{cm} in Figure 4-7.

Figure 4-7 shows the DAQPad-6020E (BNC) connector wiring.

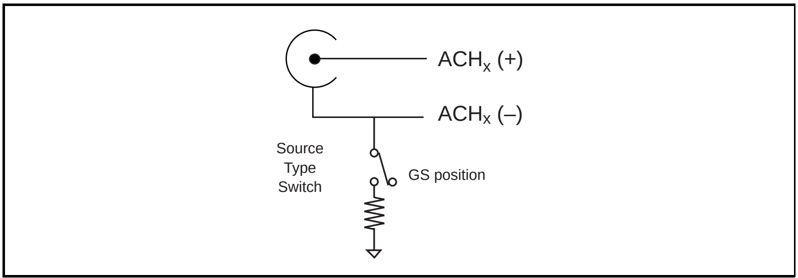


Figure 4-8. BNC Connector Wiring

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-9 shows how to connect a floating signal source to an DAQPad-6020E channel configured in DIFF input mode.

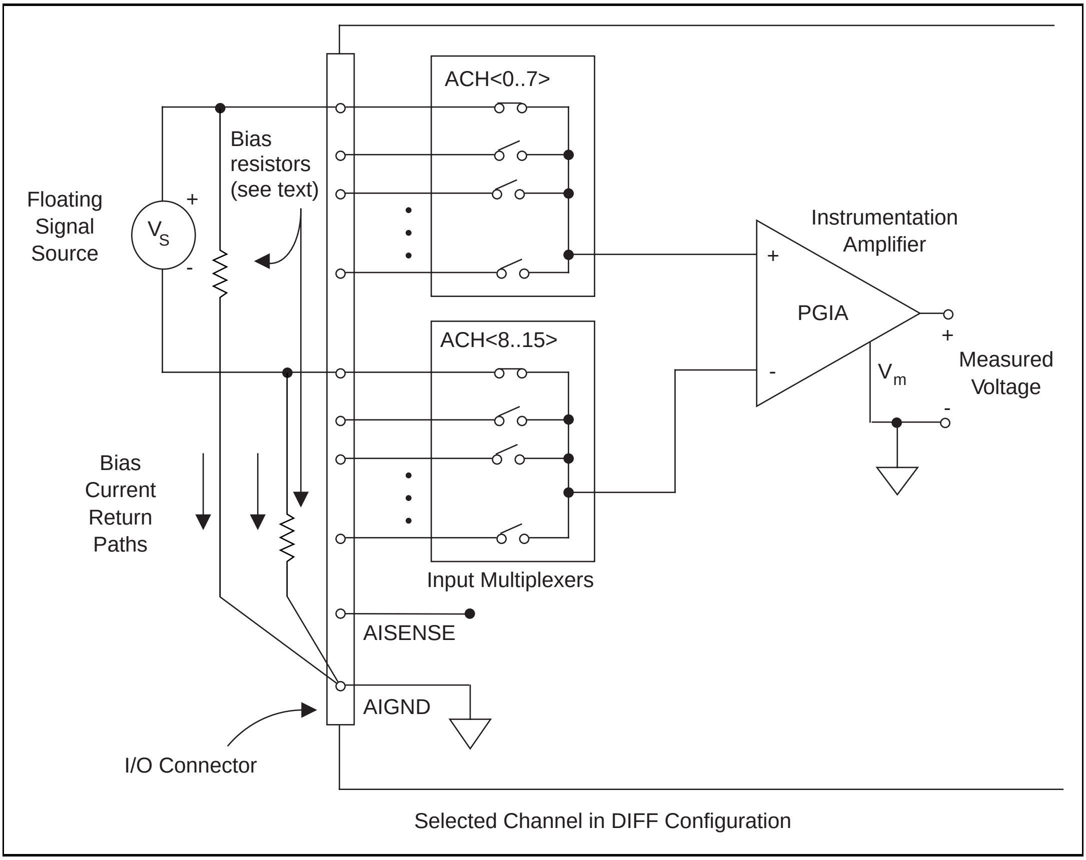


Figure 4-9. Differential Input Connections for Nonreferenced Signals

Figure 4-9 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA, and the PGIA will saturate, causing erroneous readings. You must reference the source to AIGND. The easiest way is simply to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors at all. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and so the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-9. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce -1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs; you should be aware that there is some gain error from loading down the source.

☞ **Note** ***The DAQPad-6020E (BNC) has built-in bias resistors. These bias resistors are connected between negative terminals of the differential channels and AIGND via mechanical switches. Flip the switch(es) to the FS position for measuring floating signal sources. Refer to Figure 4-5 for more information.***

Single-Ended Connection Considerations

A single-ended connection is one in which the DAQPad-6020E analog input signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 analog input channels are available.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the DAQPad-6020E are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

You can software configure the DAQPad-6020E channels for two different types of single-ended connections—RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources; in this case, the DAQPad-6020E provides the reference ground point for the external signal. The NRSE input configuration is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the DAQPad-6020E should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Note ***Refer to Appendix C,*** *Measuring More than Eight Channels with the DAQPad-6020E (BNC)* ***for single-ended input considerations with the DAQPad-6020E (BNC).***

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-10 shows how to connect a floating signal source to an DAQPad-6020E channel configured for RSE mode.

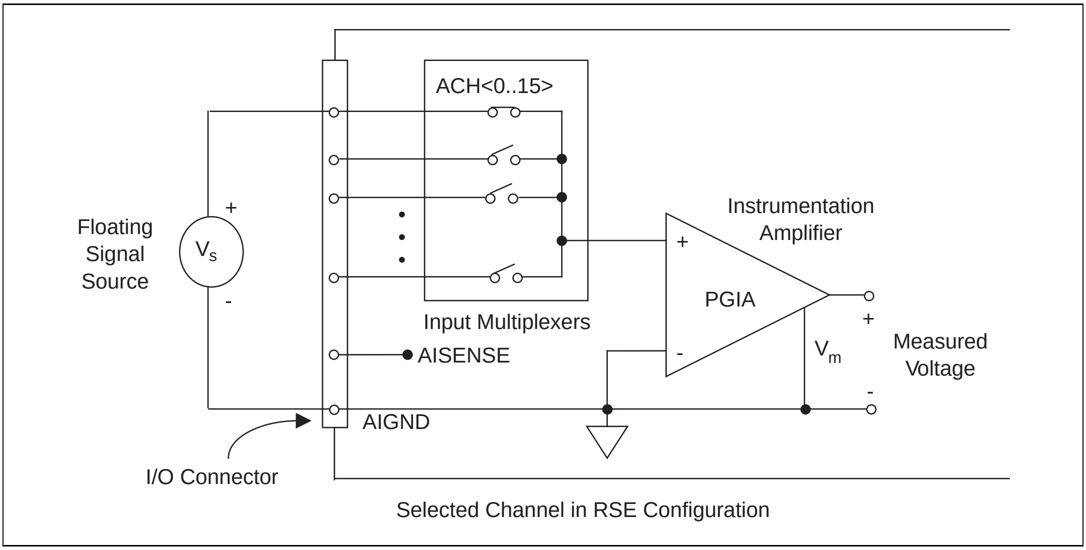


Figure 4-10. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure your DAQPad-6020E in the NRSE input configuration. The signal is then connected to the positive input of the DAQPad-6020E PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the DAQPad-6020E ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of an DAQPad-6020E were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-11 shows how to connect a grounded signal source to a DAQPad-6020E channel configured for NRSE mode.

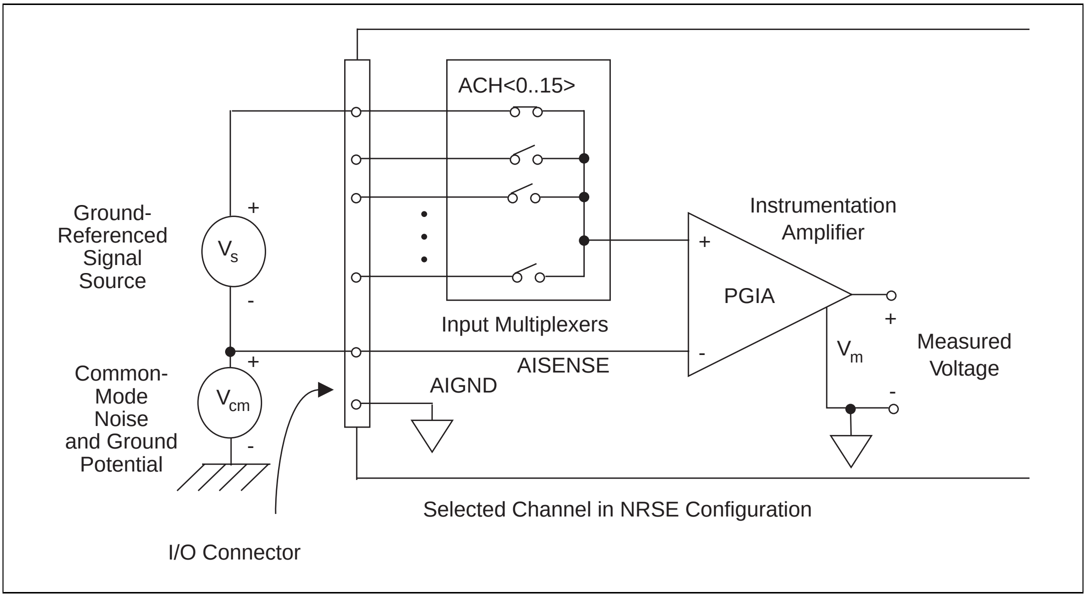


Figure 4-11. Single-Ended Input Connections for Ground-Referenced Signal

Common-Mode Signal Rejection Considerations

Figures 4-7 and 4-11 show connections for signal sources that are already referenced to some ground point with respect to the DAQPad-3006E. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as V^{+}_{in} and V^{-}_{in} are both within ±11 V of AIGND.

Analog Output Signal Connections

The analog output signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND.

DAC0OUT is the voltage output signal for analog output channel 0. DAC1OUT is the voltage output signal for analog output channel 1.

EXTREF is the external reference input for both analog output channels. You must configure each analog output channel individually for external reference selection in order for the signal applied at the external reference input to be used by that channel. If you do not specify an external reference, the channel will use the internal reference. Analog output configuration options are explained in the *Analog Output* section in Chapter 3, *Hardware Overview*. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both analog output channels and the external reference signal.

Figure 4-12 shows how to make analog output connections and the external reference input connection to your DAQPad-6020E.

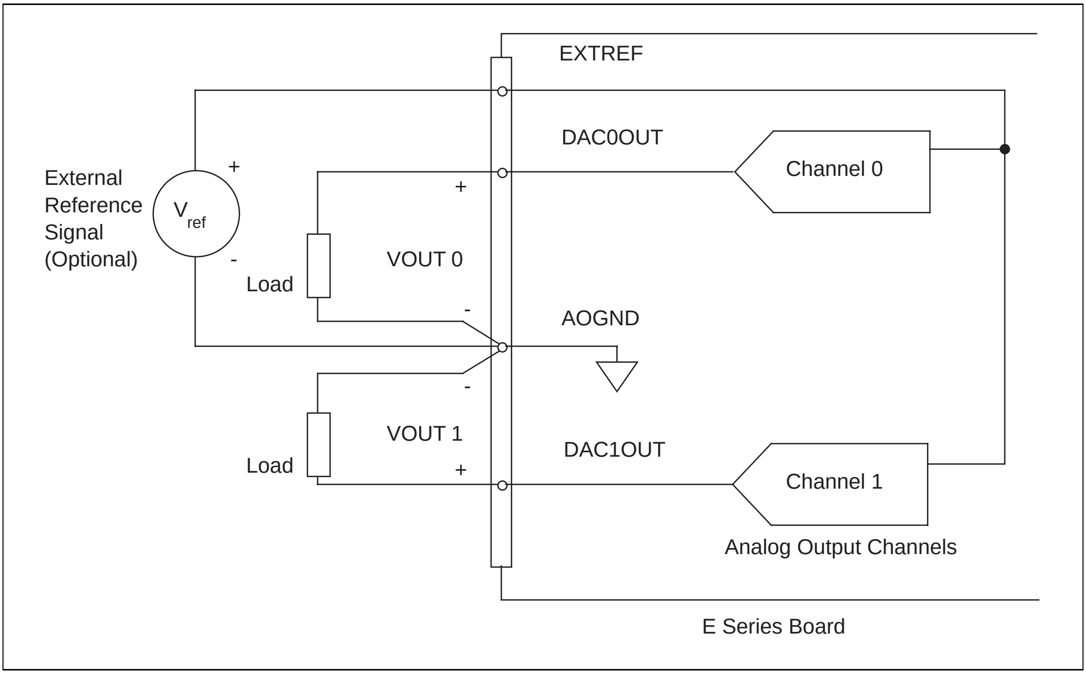


Figure 4-12. Analog Output Connections

The external reference signal can be either a DC or an AC signal. The device multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Timing Connections

⚠ **Caution** ***Exceeding the maximum input voltage ratings, which are listed in Table 4-1, can damage the DAQPad-6020E and the PC. National Instruments is NOT liable for any damages resulting from such signal connections.***

All external control over the timing of your DAQPad-6020E is routed through the 10 programmable function inputs labeled PFI0 through PFI9. These signals are explained in detail in the next section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many data acquisition, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any data acquisition, waveform generation, and general-purpose timing signals.

The data acquisition signals are explained in the *Data Acquisition Timing Connections* section later in this chapter. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section later in this chapter. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section later in this chapter.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-13, which shows how to connect an external TRIG1 source and an external CONVERT* source to two of the DAQPad-6020E PFI pins.

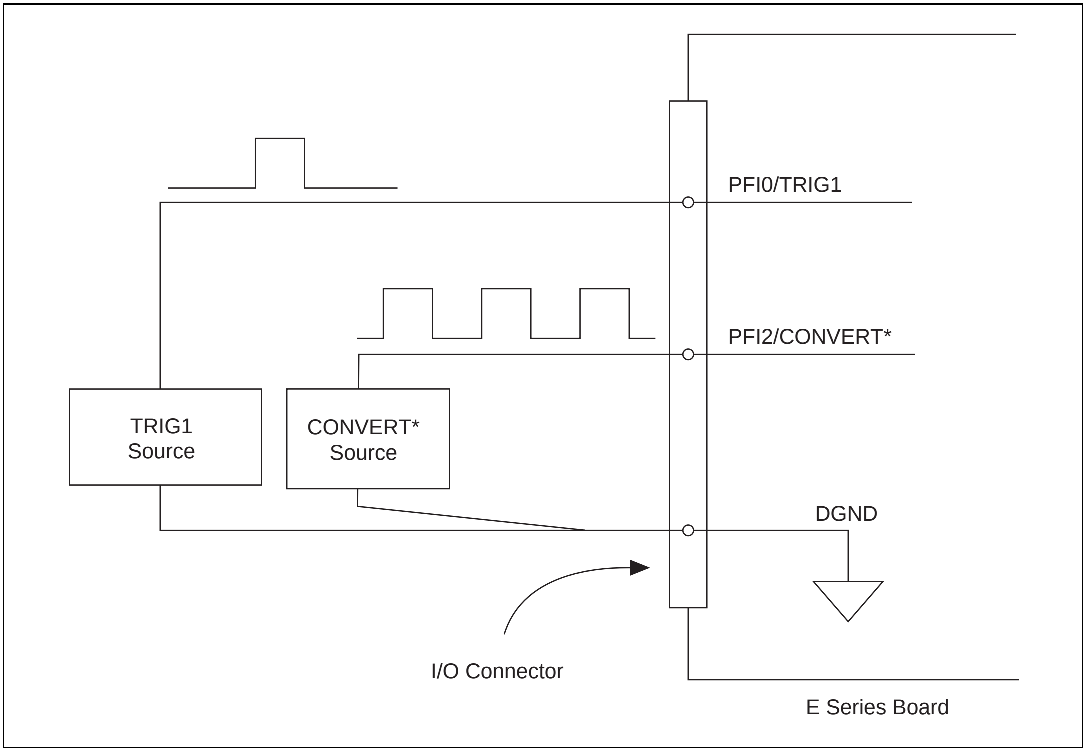


Figure 4-13. Timing I/O Connections

Programmable Function Input Connections

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. You must be careful not to drive a PFI signal externally when it is configured as an output.

As an input, you can individually configure each PFI for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection will depend upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there may be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

Data Acquisition Timing Connections

The data acquisition timing signals are SCANCLK, EXTSTROBE*, TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, and SISOURCE.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered data acquisition sequence is shown in Figure 4-14. Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-15 shows a typical pretriggered data acquisition sequence. The description for each signal shown in these figures is included later in this chapter.

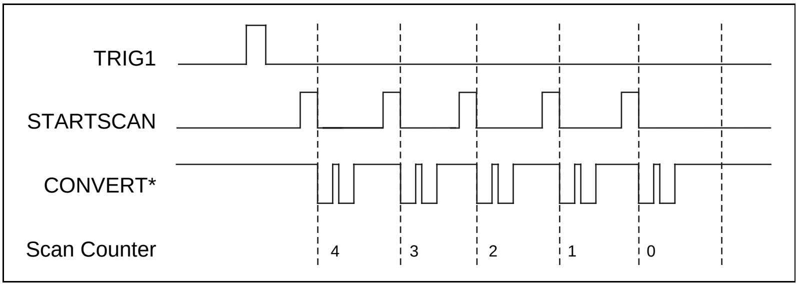


Figure 4-14. Typical Posttriggered Acquisition

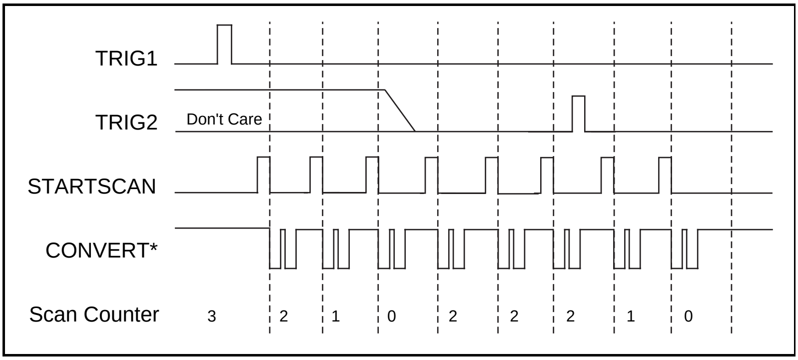


Figure 4-15. Typical Pretriggered Acquisition

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software selectable but is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-16 shows the timing for the SCANCLK signal.

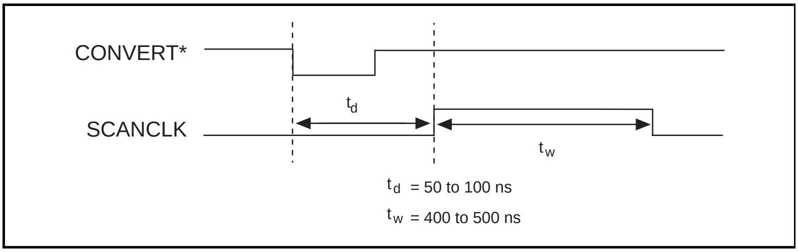


Figure 4-16. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-17 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

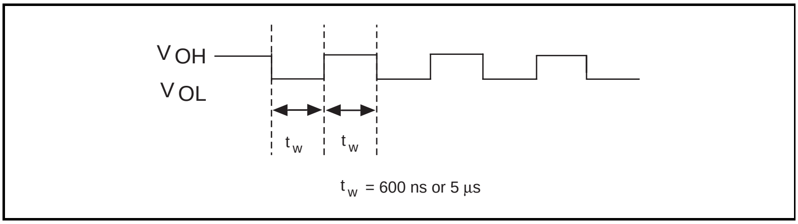


Figure 4-17. EXTSTROBE* Signal Timing

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-14 and 4-15 for the relationship of TRIG1 to the data acquisition sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the data acquisition sequence for both posttriggered and pretriggered acquisitions. See Chapter 3 for more information on analog triggering.

As an output, the TRIG1 signal reflects the action that initiates a data acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-18 and 4-19 show the input and output timing requirements for the TRIG1 signal.

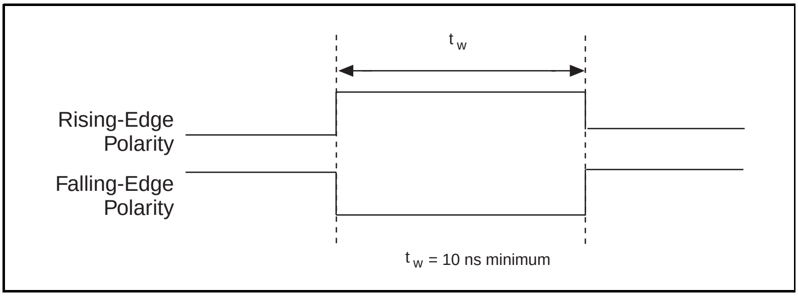


Figure 4-18. TRIG1 Input Signal Timing

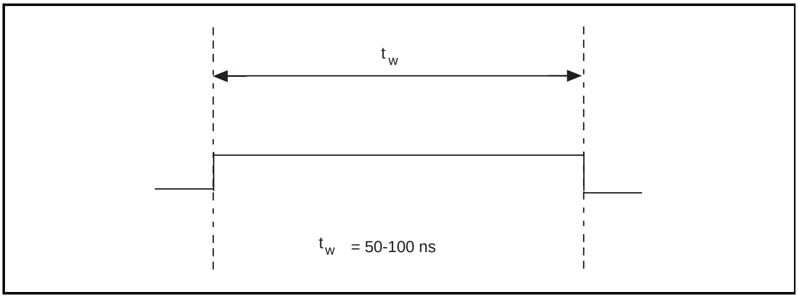


Figure 4-19. TRIG1 Output Signal Timing

The device also uses the TRIG1 signal to initiate pretriggered data acquisition operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered data acquisition operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin.

Refer to Figure 4-16 for the relationship of TRIG2 to the data acquisition sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG2 signal initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the device will acquire a fixed number of scans and the acquisition will stop. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-20 and 4-21 show the input and output timing requirements for the TRIG2 signal.

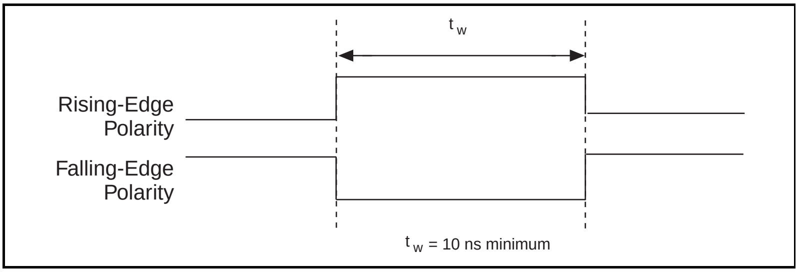


Figure 4-20. TRIG2 Input Signal Timing

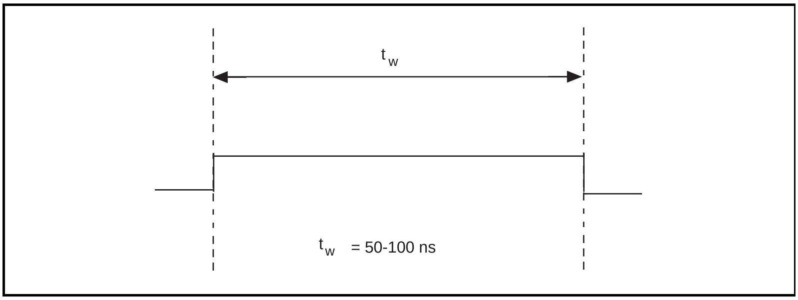


Figure 4-21. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin.

Refer to Figures 4-16 and 4-17 for the relationship of STARTSCAN to the data acquisition sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter is started if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan. This is true even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN will be deasserted t_{off} after the last conversion in the scan is initiated. This output is set to tri-state at startup.

Figures 4-22 and 4-23 show the input and output timing requirements for the STARTSCAN signal

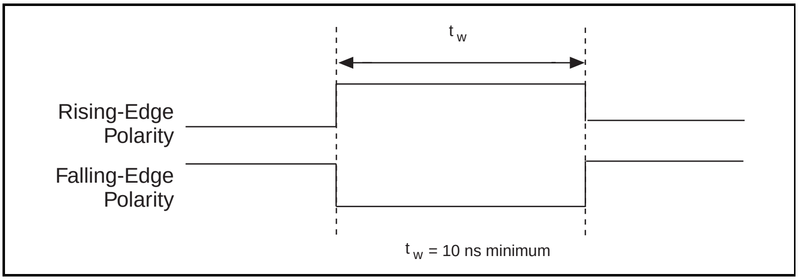


Figure 4-22. STARTSCAN Input Signal Timing

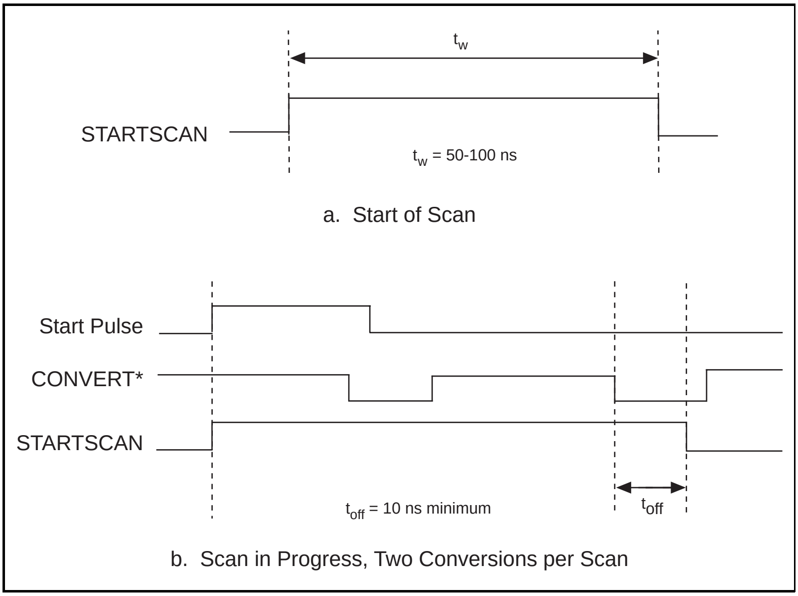


Figure 4-23. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* will appear when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN will generate a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on your DAQPad-6020E internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a data acquisition sequence. Scans occurring within a data acquisition sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-16 and 4-17 for the relationship of CONVERT* to the data acquisition sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC. This is true even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-24 and 4-25 show the input and output timing requirements for the CONVERT* signal.

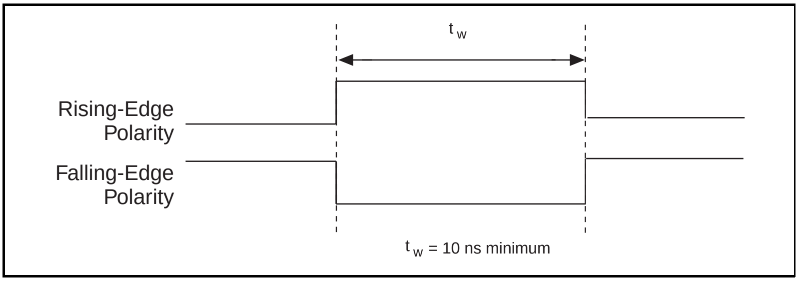


Figure 4-24. CONVERT* Input Signal Timing

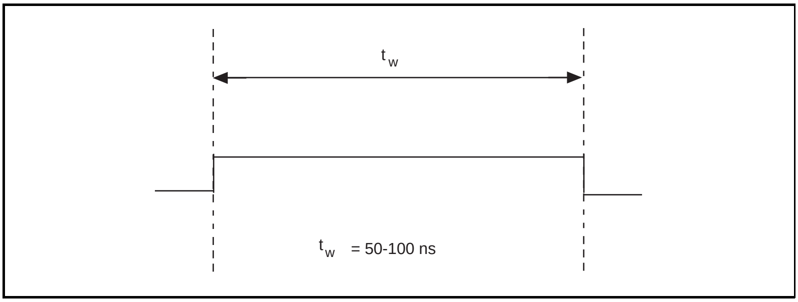


Figure 4-25. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The sample interval counter on the DAQPad-6020E normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in readiness for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a data acquisition sequence. Scans occurring within a data acquisition sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a data acquisition sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-26 shows the timing requirements for the SISOURCE signal.

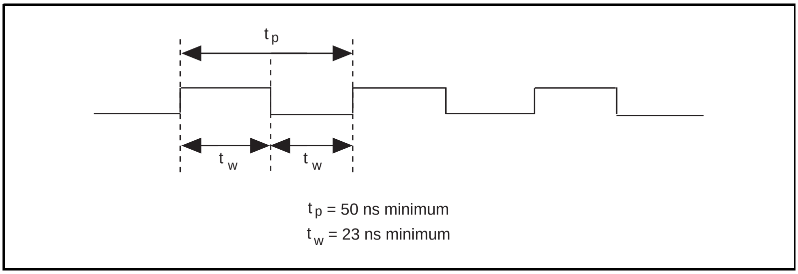


Figure 4-26. SISOURCE Signal Timing

Waveform Generation Timing Connections

The analog group defined for your DAQPad-6020E is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the

WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation. This is true even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-27 and 4-28 show the input and output timing requirements for the WFTRIG signal.

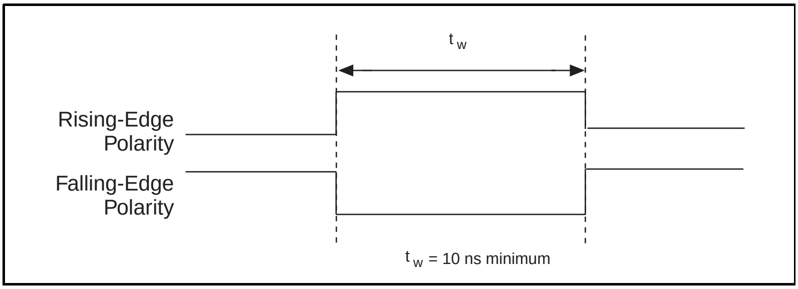


Figure 4-27. WFTRIG Input Signal Timing

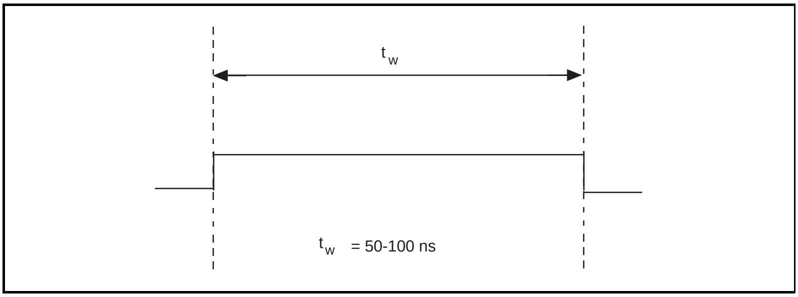


Figure 4-28. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs. This is true even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to tri-state at startup.

Figures 4-29 and 4-30 show the input and output timing requirements for the UPDATE* signal.

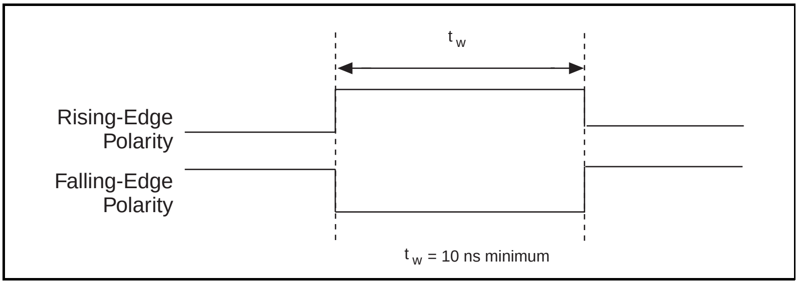


Figure 4-29. UPDATE* Input Signal Timing

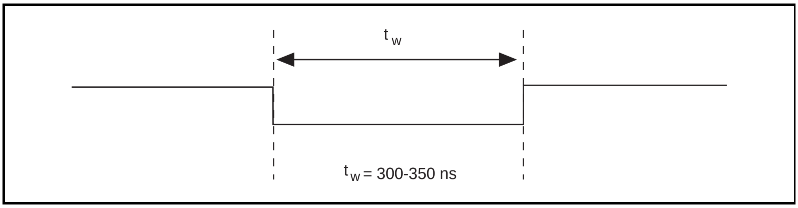


Figure 4-30. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The DAQPad-6020E UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-31 shows the timing requirements for the UISOURCE signal.

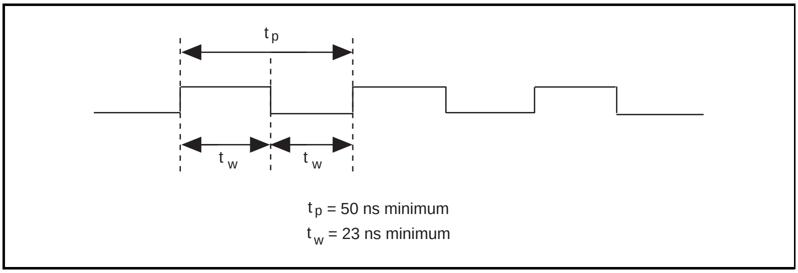


Figure 4-31. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0. This is true even if another PFI is externally inputting the source clock. This output is set to tri-state at startup.

Figure 4-32 shows the timing requirements for the GPCTR0_SOURCE signal.

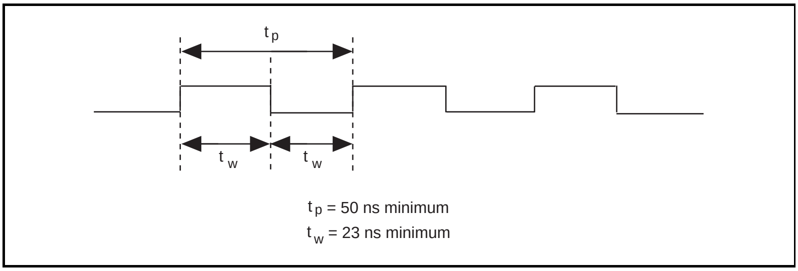


Figure 4-32. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-33 shows the timing requirements for the GPCTR0_GATE signal.

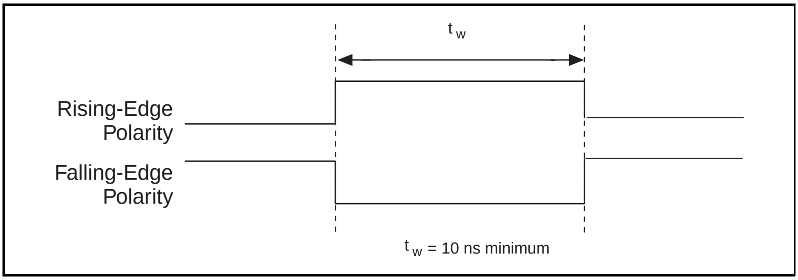


Figure 4-33. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options— pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-34 shows the timing of the GPCTR0_OUT signal.

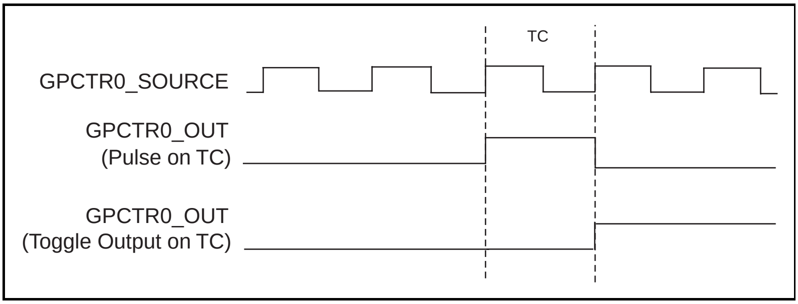


Figure 4-34. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 will count down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1. This is true even if the source clock is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-35 shows the timing requirements for the GPCTR1_SOURCE signal.

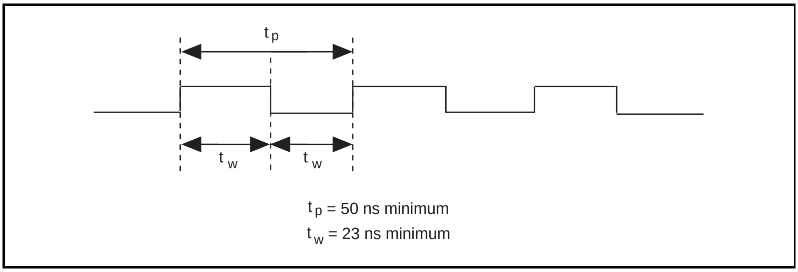


Figure 4-35. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-36 shows the timing requirements for the GPCTR1_GATE signal.

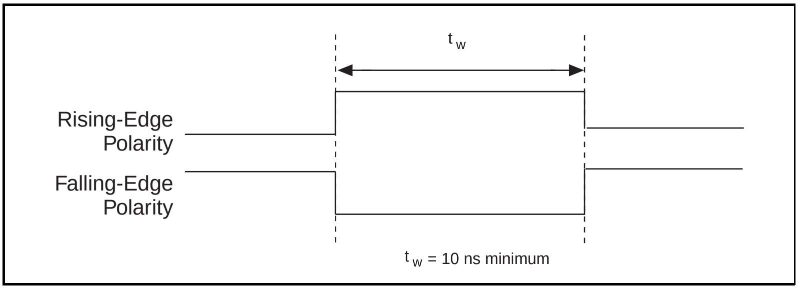


Figure 4-36. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-37 shows the timing requirements for the GPCTR1_OUT signal.

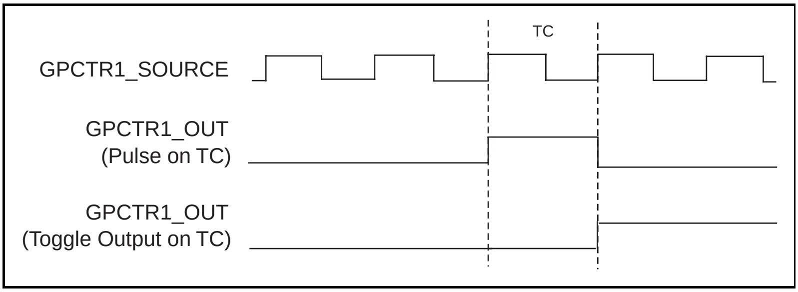
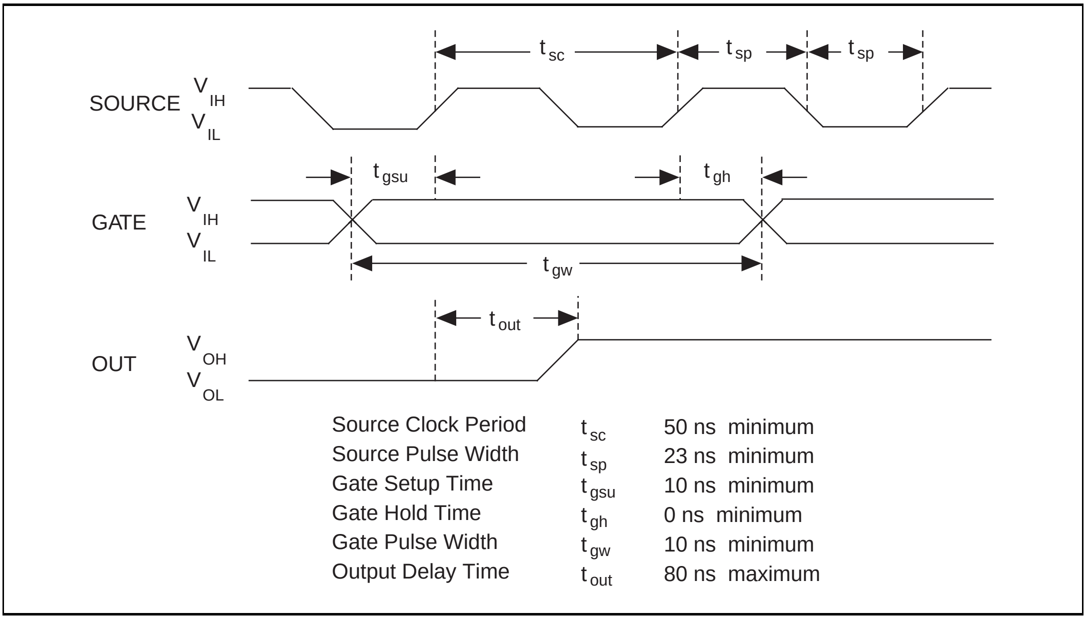


Figure 4-37. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-38 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of your DAQPad-6020E.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-38. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-38 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on your DAQPad-6020E. Figure 4-38 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-38. The gate signal is not required to be held after the active edge of the source signal.

If an internal timebase clock is used, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the DAQPad-6020E. Figure 4-38 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The FREQ_OUT signal is the output of the DAQPad-6020E frequency generator. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This output is set to tri-state at startup.

Power Connections

Two pins on the I/0 connector supply +5 V from the PC power supply via a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry.The power rating is+4.65 VDC to +5.25 VDC at 1 A combined total for both pins

Caution ***Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the DAQPad-6020E or any other device. Doing so can damage the DAQPad-6020E and the PC. National Instruments is NOT liable for damages resulting from such a connection.***

Digital I/O Signal Connections

The digital I/O signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs.

Caution ***Exceeding the maximum input voltage ratings, which are listed in Table 4-1, can damage the DAQPad-6020E and the PC. National Instruments is NOT liable for any damages resulting from such signal connections.***

Figure 4-39 shows signal connections for three typical digital I/O applications.

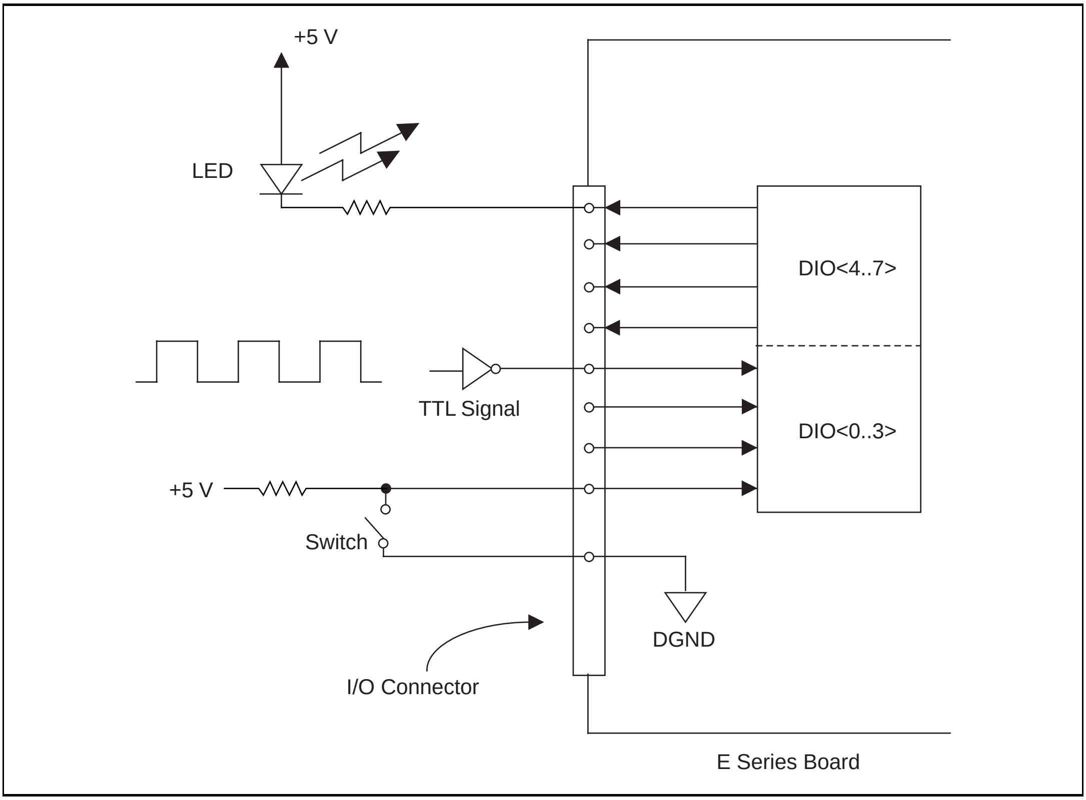


Figure 4-39. Digital I/O Connections

Figure 4-39 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices such as the LED shown in the figure.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with your DAQPad-6020E if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to analog input signal routing to the device, although they also apply to signal routing in general.

You can minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the device. With this type of wire, the signals attached to the CH+ and CH- inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PC DAQ system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to your DAQPad-6020E:

- Separate DAQPad-6020E signal lines from high-current or high-voltage lines. These lines are capable of inducing currents in or voltages on the DAQPad-6020E signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the application note, *Field Wiring and Noise Consideration for Analog Signals*, available from National Instruments.

5

Calibration

This chapter discusses the calibration procedures for your DAQPad-6020E. If you are using the NI-DAQ driver software, it includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the DAQPad-6020E, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for all but the most forgiving applications. If no device calibration were performed, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you, and these are described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

Your DAQPad-6020E is factory calibrated before shipment at approximately 25° C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM, there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it will be used.

Self-Calibration

Your DAQPad-6020E can measure and correct for almost all of its calibration-related errors without any external signal connections. Your National Instruments software provides a self-calibration method you can use. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. You should initiate self-calibration to ensure that the effects of any offset, gain, and linearity drifts, particularly those due to warm-up, are minimized.

Immediately after self-calibration, the only significant residual calibration error might be gain error due to time or temperature drift of the onboard voltage reference. You can address this error by using external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount[1] of gain error, and self-calibration should be sufficient.

External Calibration

Your DAQPad-6020E has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate your device.

An external calibration refers to calibrating your device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate your device by calling the NI-DAQ calibration function.

To externally calibrate your device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. For example, to calibrate a 12-bit device, the external

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[1] Gain temperature coefficient of onboard reference is 5 ppm/° C max. For a 10° C change in operating temperature from factory calibration temperature, the gain error due to temperature drift is 50 ppm (.005%) or about 0.2 LSB max after self-calibration.

reference should be at least ±0.005% (±50 ppm) accurate. To calibrate a 16-bit device, the external reference should be at least ±0.001% (±10 ppm) accurate.

Other Considerations

The CalDACs adjust the gain error of each analog output channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the analog output gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the analog output channel either in software or with external hardware. See Appendix A, *Specifications*, for analog output gain error information.

A

Specifications

This appendix lists the specifications of the DAQPad-6020E. These specifications are typical at 25° C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels	16 single-ended or 8 differential, software selectable
Type of ADC	Successive approximation
Resolution	12 bits, 1 in 4,096
Max sampling rate	100 kS/s guaranteed

Input signal ranges

Device Gain (Software Selectable)	**Device Range (Software Selectable)**	
	±5 V	**0-10 V**
.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

Input coupling .... DC

Max working voltage
(signal + common mode) .... Each input should remain within ±11 V of ground

Overvoltage protection .... ±35 V powered on, ±25 V powered off
Inputs protected .... ACH<0..15>, AISENSE

FIFO buffer size .... 4,096 samples

Data transfers .... Interrupt, programmed I/O

Configuration memory size .... 512 words

Transfer Characteristics

Relative accuracy .... ±0.2 LSB typ dithered, ±1.5 LSB max undithered

DNL .... ±0.2 LSB typ, ±1 LSB max

No missing codes .... 12 bits, guaranteed

Offset error
Pregain error after calibration...... ±2 µV max
Pregain error before calibration ... ±24 mV max
Postgain error after calibration .... ±0.5 mV max
Postgain error before calibration.. ±100 mV max

Gain error (relative to calibration reference)
After calibration (Gain = 1) .... ±0.02% of reading max
Before calibration .... ±2.0% of reading max
Gain ≠ 1 with gain error
adjusted to 0 at gain = 1............ ±0.05% of reading max

Amplifier Characteristics

Input impedance

68 pin I/O connector ....100 GΩ in parallel with 50 pf

BNC version

Powered ON

CH+ (ACH0, ACH1..ACH7)..100 GΩ in parallel with 50 pf

CH– (ACH8, ACH9..ACH15)..100 GΩ in parallel with 50 pf with built-in bias resistor disengaged or 100 Ω in parallel with 50 pf with built-in bias resistor engaged (factory default).

Powered off..................................3 kΩ min

Overload ....3 kΩ min

Input bias current................................±200 pA

Input offset current ....±100 pA

CMRR (all input ranges).....................90 dB, DC to 60 Hz

Dynamic Characteristics

Bandwidth

Small signal (–3 dB) ....150 kHz

Large signal (1% THD)................200 kHz

Settling time for full-scale step ....10 µs max to ±0.5 LSB accuracy

System noise (not including quantization)

Gain	Noise, Dither Off	Noise, Dither On
0.5 to 10	0.07 LSB rms	0.5 LSB rms
20	0.12 LSB rms	0.5 LSB rms
50	0.25 LSB rms	0.6 LSB rms
100	0.5 LSB rms	0.7 LSB rms

Crosstalk..–70 dB, DC to 100 kHz

Stability

Recommended warm-up time	30 min
Offset temperature coefficient	
Pregain	±15 µV/°C
Postgain	±240 µV/°C
Gain temperature coefficient	±20 ppm/°C
Onboard calibration reference	
Level	5.000 V (±2.5 mV) (actual value stored in EEPROM)
Temperature coefficient	±5 ppm/°C max
Long-term stability	±15 ppm $\sqrt{1, 000 \text{ h}}$

Analog Output

Output Characteristics

Number of channels	2 voltage
Resolution	12 bits, 1 in 4,096
Max update rate	20 S/s (system dependant)
Type of DAC	Double buffered, multiplying
FIFO buffer size	None
Data transfers	Interrupt, programmed I/O

Transfer Characteristics

Relative accuracy (INL)	
After calibration	±0.3 LSB typ, ±0.5 LSB max
Before calibration	±4 LSB max
DNL	
After calibration	±0.3 LSB typ, ±1.0 LSB max
Before calibration	±3 LSB max

Monotonicity	12 bits, guaranteed after calibration
Offset error	
After calibration	±1.0 mV max
Before calibration	±200 mV max
Gain error (relative to internal reference)	
After calibration	±0.01% of output max
Before calibration	±0.5% of output max
Gain error (relative to external reference)	0% to +0.5% of output max, not adjustable

Voltage Output

Ranges	±10 V, 0 to 10 V, ±EXTREF, 0 to EXTREF (software selectable)
Output coupling	DC
Output impedance	0.1 Ω max
Current drive	±5 mA max
Protection	Short-circuit to ground
Power-on state	0 V
External reference input	
Range	±11 V
Overvoltage protection	±35 V powered on, ±25 V powered off
Input impedance	10 kΩ
Bandwidth (–3 dB)	300 kHz

Dynamic Characteristics

Settling time for full-scale step	10 µs to ±0.5 LSB accuracy
Slew rate	10 V/µs

Noise .... 200 μV_{rms}, DC to 1 MHz

Glitch energy (at midscale transition)

Magnitude .... ±100 mV

Duration .... 3 µs

Stability

Offset temperature coefficient........... ±50 µV/°C

Gain temperature coefficient

Internal reference......................... ±25 ppm/°C

External reference .... ±25 ppm/°C

Onboard calibration reference

Level .... 5.000 V(±2.5 mV) (actual value stored in EEPROM)

Temperature coefficient.............. ±5 ppm/°C max

Long-term stability .... ±15 ppm $\sqrt{1,000\ h}$

Digital I/O

Number of channels .... 8 input/output

Compatibility .... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	-320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Data transfers .... Programmed I/O

Timing I/O

Number of channels	2 up/down counter/timers, 1 frequency scaler
Resolution	
Counter/timers	24 bits
Frequency scalers	4 bits
Compatibility	TTL/CMOS
Base clocks available	
Counter/timers	20 MHz, 100 kHz
Frequency scaler	10 MHz, 100 kHz
Base clock accuracy	±0.01%
Max source frequency	20 MHz
Min source pulse duration	10 ns in edge-detect mode
Min gate pulse duration	10 ns in edge-detect mode
Data transfers	Interrupts, programmed I/O

Triggers

Digital Trigger

Compatibility	TTL
Response	Rising or falling edge
Pulse width	10 ns min

Bus Interface

Type	USB high speed

Power Requirement

9 to 30 VDC	15 W

☞ **Note** ***Power supply voltage should never go below 8.5 V, including AC ripple.***

Power available at I/O connector	+4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions	
Half-size Box (68-pin I/O connector)	14.6 by 21.3 by 3.8 cm (5.8 by 8.4 by 1.5 in.)
Full-size Box (not including BNC connector)	30.7 by 25.4 by 4.3 cm (12.1 by 10 by 1.7 in.)
Weight	0.82 kg (1.8 lb)
I/O connector	68-pin male SCSI-II type

Environment

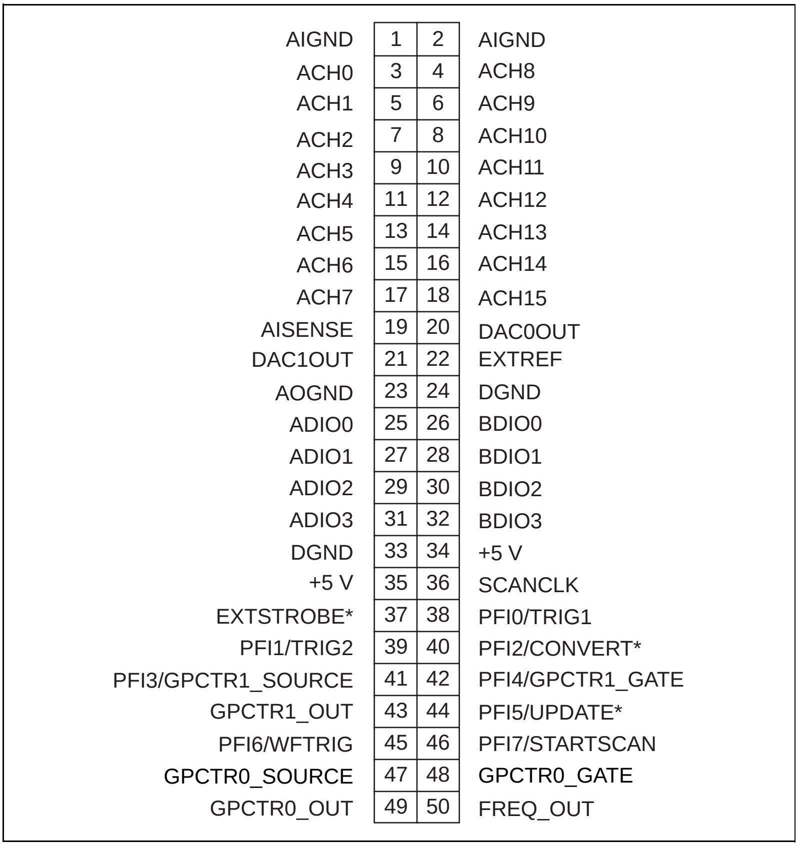
Operating temperature	0° to 50° C
Storage temperature	–55° to 150°C
Relative humidity	5% to 90% noncondensing

B

Optional Cable Connector Descriptions

This appendix describes the connectors on the optional cables for the DAQPad-6020E.

Figure B-1 shows the pin assignments for the 50-pin MIO connector.



AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
ADIO0	25	26	BDIO0
ADIO1	27	28	BDIO1
ADIO2	29	30	BDIO2
ADIO3	31	32	BDIO3
DGND	33	34	+5 V
+5 V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
GPCTR0_SOURCE	47	48	GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

Figure B-1. SH6850 or R6850 MIO Connector Pin Assignments

Figure B-2 shows the pin assignments for the 68-pin MIO connector.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT	22	56	AIGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

Figure B-2. 68-Pin MIO Connector Pin Assignments

C

Measuring More than Eight Channels with the DAQPad-6020E (BNC)

This appendix explains how to measure more than eight channels with the DAQPad-6020E (BNC). If you are measuring eight channels or less, you do not need to read this section.

The DAQPad-6020E (BNC) is designed for convenient measurement of up to eight differential channels using BNC connectors and cabling. In certain situations, however, it may be desirable to increase the channel count beyond eight. In this case, you must use one of the single-ended measurement modes with the DAQPad-6020E (BNC). Up to 16 single-ended channels are available in the single-ended measurement configuration.

Single-ended measurement modes require changing the source type switch (S0 through S7) settings. Figure C-1 shows the ground-referenced resistor switch settings.

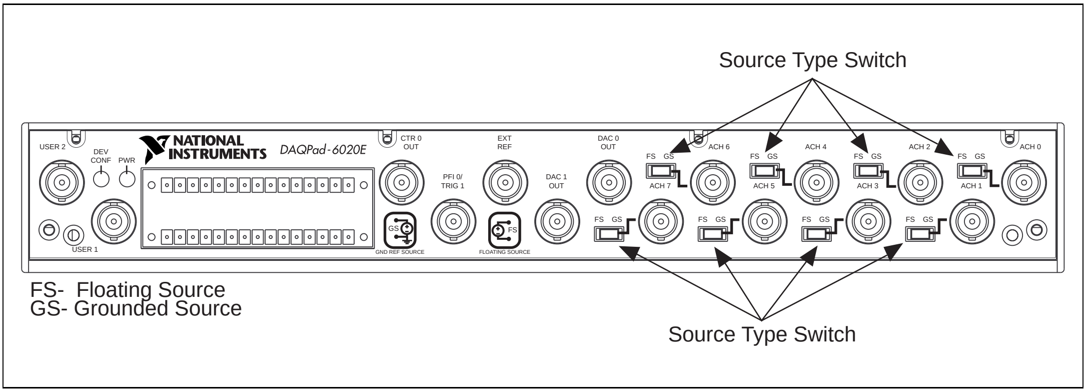


Figure C-1. DAQPad-6020E (BNC) Front Panel

The switches S0 through S7 should be set to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector to ground, allowing it to be used as a single-ended channel. For example, BNC connector labeled CH0, provides access to 2 single-ended channels, ACH0 and ACH8, if the front panel switch is set to GS and the board is configured in single-ended input configuration via software.

D

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your DAQPad-6020E.

General Information

1. **What is a DAQPad-6020E?**

   The DAQPad-6020E is a USB platform, enhanced MIO device that uses the DAQ-STC for timing.

2. **What is the DAQ-STC?**

   The DAQ-STC is the new system timing control ASIC (application-specific integrated circuit) designed by National Instruments and is the backbone of the DAQPad-6020E. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into three groups:

   - Analog input—two 24-bit, two 16-bit counters
   - Analog output—three 24-bit, one 16-bit counters
   - General-purpose counter/timer functions—two 24-bit counters

   The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate are possible.

3. **What type of 5 V protection does the DAQPad-6020E have?**

   The DAQPad-6020E has 5 V lines equipped with a self-resetting 1 A fuse.

Installation and Configuration

4. **How do I know if my version of Windows supports USB?**

   Look in the **System** properties in the control panel. The **Device Manager** tab should list a **Universal Serial Bus Controller** along with a USB Controller and a USB root hub. If your computer has this and also USB ports, your machine is supported. If your computer has USB ports but no controller is listed in the **Device Manager**, you might need to upgrade your software.

5. **What is the best way to test my device without having to program the device?**

   The NI-DAQ Configuration Utility has a **Test** panel with some excellent tools for doing simple functional tests of the device, such as analog input and output, digital I/O, and counter/timer tests.

6. **What does the blink pattern mean for the configuration LED on the front panel?**

   This LED blinks to indicate the status of the DAQPad-6020E. It also can indicate an error through a blink code. Refer to Table 2-1 for more information.

Analog Input and Output

7. **I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?**

   When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of your output signal.

8. **Can I synchronize a one-channel analog input data acquisition with a one-channel analog output waveform generation on my DAQPad-6020E?**

   Yes. One way to accomplish this is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps a through d below, in addition to the instructions for data acquisition and waveform generation configuration found in the *NI-DAQ Function Reference Manual for PC Compatibles*.

   a. Enable the PFI5 line for output, as follows:

      - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW)`.
      - If you are using LabVIEW, invoke the Route Signal VI with **signal name** set to PFI5 and **signal source** set to AO Update.

   b. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:

      - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW)`.
      - If you are using LabVIEW, invoke the AI Clock Config VI with **clock source code** set to PFI pin, high to low, and **clock source string** set to 5.

   c. Initiate analog input data acquisition, which will start only when the analog output waveform generation starts.

      - If you are using NI-DAQ, call `DAQ_Start (deviceNumber, chan, gain, buffer, count, timebase, sampInterval)`.
      - If you are using LabVIEW, invoke the AI Control VI with **control code** set to 0 (start).

   d. Initiate analog output waveform generation.

      If you are using NI-DAQ, call `WFM_Group_Control` with **operation** set to 1 (start).

      If you are using LabVIEW, invoke the AO Control VI with **control code** set to 0 (start).

Timing and Digital I/O

9. **What types of triggering can be implemented in hardware on my DAQPad-6020E?**

   The DAQPad-6020E hardware supports digital triggering.

10. **What added functionality does the DAQ-STC make possible in contrast to the Am9513?**

    The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

11. **What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?**

    The DAQ-STC-based MIO devices have a 20 MHz timebase. The Am9513-based MIO devices have a 1 MHz or 5 MHz timebase.

12. **The counter/timer examples supplied with NI-DAQ are not compatible with a DAQPad-6020E. Where can I find examples to illustrate the use of the DAQ-STC as a general-purpose counter/timer?**

    If you are using the NI-DAQ language interface and a C compiler under DOS, a new subdirectory called `GPCTR`, which lies beneath the `examples` directory, contains 16 examples of the most common uses of the DAQ-STC.

13. **Will the counter/timer applications that I wrote previously work with the DAQ-STC?**

    If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs will still run. However, there are many differences in the counters between the DAQPad-6020E and other devices; the counter numbers are different, timebase selections are different, the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using the NI-DAQ language interface, or LabWindows/CVI, the answer is, no, the counter/time applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

14. **I'm using one of the general-purpose counter/timers on my DAQPad-6020E, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?**

    If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.

15. **What are the PFIs and how do I configure these lines?**

    PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

    If you are using the NI-DAQ language interface, LabWindows, or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

    If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode Config, and CTR Pulse Config advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

⚠ **Caution** ***If you enable a PFI line for output, do not connect any external signal source to it; if you do, you can damage the device, the computer, and the connected equipment.***

16. What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-1, *I/O Signal Summary*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high-impedance state after power on, and Table 4-1 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high-impedance state.

E

Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

National Instruments has technical assistance through electronic, fax, and telephone systems to quickly provide the information you need. Our electronic services include a bulletin board service, an FTP site, a fax-on-demand system, and e-mail support. If you have a hardware or software problem, first try the electronic support systems. If the information available on these systems does not answer your questions, we offer fax and telephone support through our technical support centers, which are staffed by applications engineers.

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National Instruments has BBS and FTP sites dedicated for 24-hour support with a collection of files and documents to answer most common customer questions. From these sites, you can also download the latest instrument drivers, updates, and example programs. For recorded instructions on how to use the bulletin board and FTP services and for BBS automated information, call 512 795 6990. You can access these services at:

United States: 512 794 5422
Up to 14,400 baud, 8 data bits, 1 stop bit, no parity

United Kingdom: 01635 551422
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

France: 01 48 65 15 59
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

FTP Support

To access our FTP site, log on to our Internet host, `ftp.natinst.com`, as `anonymous` and use your Internet address, such as `joesmith@anywhere.com`, as your password. The support files and documents are located in the `/support` directories.

Fax-on-Demand Support

Fax-on-Demand is a 24-hour information retrieval system containing a library of documents on a wide range of technical information. You can access Fax-on-Demand from a touch-tone telephone at 512 418 1111.

E-Mail Support (Currently USA Only)

You can submit technical support questions to the applications engineering team through e-mail at the Internet address listed below. Remember to include your name, address, and phone number so we can contact you with solutions and suggestions.

`support@natinst.com`

Telephone and Fax Support

National Instruments has branch offices all over the world. Use the list below to find the technical support number for your country. If there is no National Instruments office in your country, contact the source from which you purchased your software to obtain support.

Country	Telephone	Fax
Australia	03 9879 5166	03 9879 6277
Austria	0662 45 79 90 0	0662 45 79 90 19
Belgium	02 757 00 20	02 757 03 11
Brazil	011 288 3336	011 288 8528
Canada (Ontario)	905 785 0085	905 785 0086
Canada (Québec)	514 694 8521	514 694 4399
Denmark	45 76 26 00	45 76 26 02
Finland	09 725 725 11	09 725 725 55
France	01 48 14 24 24	01 48 14 24 14
Germany	089 741 31 30	089 714 60 35
Hong Kong	2645 3186	2686 8505
Israel	03 6120092	03 6120095
Italy	02 413091	02 41309215
Japan	03 5472 2970	03 5472 2977
Korea	02 596 7456	02 596 7455
Mexico	5 520 2635	5 520 3282
Netherlands	0348 433466	0348 430673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 200 51 51	056 200 51 55
Taiwan	02 377 1200	02 737 4644
United Kingdom	01635 523545	01635 523154
United States	512 795 8248	512 794 5678

Technical Support Form

Photocopy this form and update it each time you make changes to your software or hardware, and use the completed copy of this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name ____

Company ____

Address ____

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Fax (___)_____________________ Phone (___) ______________________________

Computer brand _________________ Model _________________ Processor_____________________

Operating system (include version number) __________________________________

Clock speed ______MHz RAM _____MB Display adapter ___________________________

Mouse ___yes ___no Other adapters installed ___________________________________

Hard disk capacity _____MB Brand ____

Instruments used ____

____

National Instruments hardware product model___________ Revision ________________________

Configuration ____

National Instruments software product ______________________________Version _____________

Configuration ____

The problem is: ____

____

____

____

____

List any error messages: ____

____

____

The following steps reproduce the problem:_____________________________________

____

____

____

____

____

DAQPad-6020E Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

National Instruments Products

DAQPad-6020E device ____________________

DAQPad-6020E serial number ____________________

Programming choice (NI-DAQ, LabVIEW, LabWindows/CVI, or other)____________________

Software version ____________________

Other Products

Computer model ____________________

Microprocessor ____________________

Clock frequency or speed ____________________

Type of video board installed ____________________

Operating system version ____________________

Operating system mode ____________________

Programming language ____________________

Programming language version ____________________

Other boards in system ____________________

Base I/O address of other boards ____________________

Documentation Comment Form

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Title: *DAQPad-6020E User Manual*

Edition Date: September 1998

Part Number: 321563A-01

Please comment on the completeness, clarity, and organization of the manual.

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If you find errors in the manual, please record the page numbers and describe the errors.

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Thank you for your help.

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
μ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

%	percent
±	plus or minus
°	degrees
/	per
+	positive of, or plus
–	negative of, or minus
Ω	ohms
$\sqrt{\quad}$	square root of
+5 V	+5 VDC source signal

A

A	amperes

AC	alternating current
AC coupled	allowing the transmission of AC signals while blocking DC signals
ACH	analog input channel signal
A/D	analog-to-digital
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADC resolution	the resolution of the ADC, which is measured in bits. An ADC with 16 bits has a higher resolution, and thus a higher degree of accuracy, than a 12-bit ADC.
address	character code that identifies a specific location (or series of locations) in memory
AIGATE	analog input gate signal
AIGND	analog input ground signal
AISENSE	analog input sense signal
AISENSE2	analog input sense 2 signal
alias	a false lower frequency component that appears in sampled data acquired at too low a sampling rate
AMD	Advanced Micro Devices
amplification	a type of signal conditioning that improves accuracy in the resulting digitized signal and reduces noise
amplitude flatness	a measure of how close to constant the gain of a circuit remains over a range of frequencies
AOGND	analog output ground signal
ASIC	application-specific integrated circuit
asynchronous	(1) hardware—a property of an event that occurs at an arbitrary time, without synchronization to a reference clock (2) software—a property of a function that begins an operation and returns prior to the completion or termination of the operation

attenuate	to decrease the amplitude of a signal
attenuation ratio	the factor by which a signal's amplitude is decreased

B

b	bit—one binary digit, either 0 or 1
B	byte—eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
bandwidth	the range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond
base address	a memory address that serves as the starting address for programmable registers. All other addresses are located by adding to the base address.
baud rate	serial communications data transmission rate expressed in bits per second (b/s)
BCD	binary-coded decimal
binary	a number system with a base of 2
BIOS	basic input/output system or built-in operating system
bipolar	a signal range that includes both positive and negative values (for example, –5 V to +5 V)
BNC	a type of coaxial signal connector
break-before-make	a type of switching contact that is completely disengaged from one terminal before it connects with another terminal
breakdown voltage	the voltage high enough to cause breakdown of optical isolation, semiconductors, or dielectric materials. *See also* working voltage.
buffer	temporary storage for acquired or generated data (software)
burst-mode	a high-speed data transfer in which the address of the data is sent followed by back-to-back data words while a physical signal is asserted

bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the AT bus, NuBus, Micro Channel, and EISA bus.
bus master	a type of a plug-in board or controller with the ability to read and write devices on the computer bus

C

C	Celsius
CalDAC	calibration DAC
cascading	process of extending the counting range of a counter chip by connecting to the next higher counter
channel	pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
channel clock	the clock controlling the time interval between individual channel sampling within a scan. Boards with simultaneous sampling do not have this clock.
circuit trigger	a condition for starting or stopping clocks
clock	hardware component that controls timing for reading from or writing to groups
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
code width	the smallest detectable change in an input voltage of a DAQ device
cold-junction compensation	a method of compensating for inaccuracies in thermocouple circuits
common-mode range	the input range over which a circuit can handle a common-mode signal
common-mode signal	the mathematical average voltage, relative to the computer’s ground, of the signals from a differential input

common-mode voltage	any voltage present at the instrumentation amplifier inputs with respect to amplifier ground
compensation range	the range of a parameter for which compensating adjustment can be made
conditional retrieval	a method of triggering in which you simulate an analog trigger using software. Also called software triggering.
conversion device	device that transforms a signal from one form to another. For example, analog-to-digital converters (ADCs) for analog input, digital-to-analog converters (DACs) for analog output, digital input or output ports, and counter/timers are conversion devices.
conversion time	the time required, in an analog input or output system, from the moment a channel is interrogated (such as with a read instruction) to the moment that accurate data is available
CONVERT*	convert signal
counter/timer	a circuit that counts external pulses or clock pulses (timing)
coupling	the manner in which a signal is connected from one location to another
CPU	central processing unit
crosstalk	an unwanted signal on one channel due to an input on a different channel
current drive capability	the amount of current a digital or analog output channel is capable of sourcing or sinking while still operating within voltage range specifications
current sinking	the ability of a DAQ board to dissipate current for analog or digital output signals
current sourcing	the ability of a DAQ board to supply current for analog or digital output signals

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current

DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
daisy-chain	a method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO boards plugged into a computer, and possibly generating control signals with D/A and/or DIO boards in the same computer
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts
DC	direct current
DC coupled	allowing the transmission of both AC and DC signals
default setting	a default parameter value recorded in the driver. In many cases, the default input of a control is a certain value (often 0) that means *use the current default setting*. For example, the default input for a parameter may be *do not change current setting*, and the default setting may be *no AMUX-64T boards*. If you do change the value of such a parameter, the new value becomes the new setting. You can set default settings for some parameters in the configuration utility or manually using switches located on the device.
device	a plug-in DAQ board, card, or pad that can contain multiple channels and conversion devices. Plug-in boards, PCMCIA cards, and devices such as the DAQPad-1200, which connects to your computer parallel port, are all examples of DAQ devices. SCXI modules are distinct from devices, with the exception of the SCXI-1200, which is a hybrid.
DGND	digital ground signal
DIFF	differential mode
differential input	an analog input consisting of two terminals, both of which are isolated from computer ground, whose difference is measured

differential measurement system	a way you can configure your device to read signals, in which you do not need to connect either input to a fixed reference, such as the earth or a building ground
digital port	See *port*.
digital trigger	a TTL level signal having two discrete levels—a high and a low level
DIO	digital input/output
DIP	dual inline package
dithering	the addition of Gaussian noise to an analog input signal
DNL	differential nonlinearity
drivers	software that controls a specific hardware device such as a DAQ board or a GPIB interface board
DSP	digital signal processing
dynamic range	the ratio of the largest signal level a circuit can handle to the smallest signal level it can handle (usually taken to be the noise level), normally expressed in decibels

E

EEPROM	electrically erasable programmable read-only memory
EMC	electromechanical compliance
encoder	a device that converts linear or rotary displacement into digital or pulse signals. The most popular type of encoder is the optical encoder, which uses a rotating disk with alternating opaque areas, a light source, and a photodetector.
EPROM	erasable programmable read-only memory—ROM that can be erased (usually by ultraviolet light exposure) and reprogrammed
ETS	equivalent-time sampling
event	the condition or state of an analog or digital signal

external trigger	a voltage pulse from an external source that triggers an event such as A/D conversion
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

false triggering	triggering that occurs at an unintended time
FIFO	first-in-first-out
filtering	a type of signal conditioning that allows you to filter unwanted signals from the signal you are trying to measure
floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
flyby	a type of high-performance data transfer in which the data bytes pass directly from the source to the target without being transferred to the controller
FREQ_OUT	frequency output signal
ft	feet

G

gain	the factor by which a signal is amplified, sometimes expressed in decibels
gain accuracy	a measure of deviation of the gain of an amplifier from the ideal gain
GATE input pin	a counter input pin that controls when counting occurs in your application
GPCTR0_GATE	general-purpose counter 0 gate signal
GPCTR1_GATE	general-purpose counter 1 gate signal
GPCTR0_OUT	general-purpose counter 0 output signal

GPCTR1_OUT	general-purpose counter 1 output signal
GPCTR0_SOURCE	general-purpose counter 0 clock source signal
GPCTR1_SOURCE	general-purpose counter 1 clock source signal
GPIB	General Purpose Interface bus, synonymous with HP-IB. The standard bus used for controlling electronic instruments with a computer. Also called IEEE 488 bus because it is defined by ANSI/IEEE Standards 488-1978, 488.1-1987, and 488.2-1987.
ground tie point	the location where two or more grounds (such as digital ground, analog output ground, analog input ground, and so on), are connected or tied together
grounded source	signal sources that are connected to ground

H

h	hour
half-flash ADC	an ADC that determines its output code by digitally combining the results of two sequentially performed, lower-resolution flash conversions
half-power bandwidth	the frequency range over which a circuit maintains a level of at least –3 dB with respect to the maximum level
handle	pointer to a pointer to a block of memory; handles reference arrays and strings. An array of strings is a handle to a block of memory containing handles to strings.
handler	a device driver that is installed as part of the operating system of the computer
handshaked digital I/O	a type of digital acquisition/generation where a device or module accepts or transfers data after a digital pulse has been received. Also called latched digital I/O.
hardware	the physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, cables, and so on
hardware triggering	a form of triggering where you set the start time of an acquisition and gather data at a known position in time relative to a trigger signal

hex	hexadecimal
Hz	hertz

I

IBM	International Business Machines
IC	integrated circuit
ID	identification
IDE	integrated development environment
immediate digital I/O	a type of digital acquisition/generation where LabVIEW updates the digital lines or port states immediately or returns the digital value of an input line. Also called nonlatched digital I/O.
in.	inches
INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry
input bias current	the current that flows into the inputs of a circuit
input impedance	the measured resistance and capacitance between the input terminals of a circuit
input offset current	the difference in the input bias currents of the two inputs of an instrumentation amplifier
instrument driver	a set of high-level software functions that controls a specific GPIB, VXI, or RS-232 programmable instrument or a specific plug-in DAQ board. Instrument drivers are available in several forms, ranging from a function callable language to a virtual instrument (VI) in LabVIEW.
instrumentation amplifier	a circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two inputs
integral control	a control action that eliminates the offset inherent in proportional control
integrating ADC	an ADC whose output code represents the average value of the input voltage over a given time interval

interrupt	a computer signal indicating that the CPU should suspend its current task to service a designated activity
interrupt level	the relative priority at which a device can interrupt
interval scanning	scanning method where there is a longer interval between scans than there is between individual channels comprising a scan
I/O	input/output
I_{OH}	current, output high
I_{OL}	current, output low
IRQ	interrupt request
ISA	Industry Standard Architecture
isolation	a type of signal conditioning in which you isolate the transducer signals from the computer for safety purposes. This protects you and your computer from large voltage spikes and makes sure the measurements from the DAQ device are not affected by differences in ground potentials.
isolation voltage	the voltage that an isolated circuit can normally withstand, usually specified from input to input and/or from any input to the amplifier output, or to the computer bus
isothermal	constructed to maintain constant temperature across area. Isothermal construction of terminal blocks increases thermocouple measurement accuracy.

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters
K	kilo—the prefix for 1,024, or 2^{10}, used with B in quantifying data or computer memory
kbytes/s	a unit for data transfer that means 1,000 or 10^3 bytes/s
kS	1,000 samples
Kword	1,024 words of memory

L

LabVIEW	laboratory virtual instrument engineering workbench
LASTCHAN	last channel (bit)
latched digital I/O	a type of digital acquisition/generation where a device or module accepts or transfers data after a digital pulse has been received. Also called handshaked digital I/O.
LED	light-emitting diode
library	a file containing compiled object modules, each comprised of one of more functions, that can be linked to other object modules that make use of these functions. NIDAQMSC.LIB is a library that contains NI-DAQ functions. The NI-DAQ function set is broken down into object modules so that only the object modules that are relevant to your application are linked in, while those object modules that are not relevant are not linked.
linearity	the adherence of device response to the equation R = KS, where R = response, S = stimulus, and K = a constant
linearization	a type of signal conditioning in which software linearizes the voltage levels from transducers, so the voltages can be scaled to measure physical phenomena
listener	a device on the GPIB that receives information from a Talker on the bus
low frequency corner	in an AC-coupled circuit, the frequency below which signals are attenuated by at least 3 dB
LSB	least significant bit

M

m	meters
M	(1) Mega, the standard metric prefix for 1 million or 10^6, when used with units of measure such as volts and hertz; (2) mega, the prefix for 1,048,576, or 2^{20}, when used with B to quantify data or computer memory
MB	megabytes of memory

Mbytes/s	a unit for data transfer that means 1 million or 10^6 bytes/s
memory buffer	See *buffer*.
MIO	multifunction I/O
MITE	MXI Interfaces to Everything is a custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high speed data transfers over the PCI bus.
MS	million samples
MSB	most significant bit
MTBF	mean time between failure
multiplexed mode	an SCXI operating mode in which analog input channels are multiplexed into one module output so that your cabled DAQ device has access to the module's multiplexed output as well as the outputs on all other multiplexed modules in the chassis through the SCXI bus. Also called serial mode.
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel

N

NC	normally closed, or not connected
NI-DAQ	National Instruments driver software for DAQ hardware
NIST	National Institute of Standards and Technology
nodes	execution elements of a block diagram consisting of functions, structures, and subVIs
noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

nonlatched digital I/O	a type of digital acquisition/generation where software updates the digital lines or port states immediately or returns the digital value of an input line. Also called immediate digital I/O or non-handshaking.
nonreferenced signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called floating signal sources. Some common example of nonreferenced signal sources are batteries, transformers, or thermocouples.
NRSE	nonreferenced single-ended mode
Nyquist Sampling Theorem	a law of sampling theory stating that if a continuous bandwidth-limited signal contains no frequency components higher than half the frequency at which it is sampled, then the original signal can be recovered without distortion

O

onboard channels	channels provided by the plug-in DAQ board
operating system	base-level software that controls a computer, runs programs, interacts with users, and communicates with installed hardware or peripheral devices
OUT	output
output settling time	the amount of time required for the analog output voltage to reach its final value within specified limits
output slew rate	the maximum rate of change of analog output voltage from one level to another

P

parallel mode	a type of SCXI operating mode in which the module sends each of its input channels directly to a separate analog input channel of the device to the module
passband	the range of frequencies which a device can properly propagate or measure

pattern generation	a type of handshaked (latched) digital I/O in which internal counters generate the handshaked signal, which in turn initiates a digital transfer. Because counters output digital pulses at a constant rate, this means you can generate and retrieve patterns at a constant rate because the handshaked signal is produced at a constant rate.
PC	personal computer
PC Card slot	a credit-card-sized expansion card that fits in a PCMCIA, often referred to as a PCMCIA card
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PCMCIA	an expansion bus architecture that has found widespread acceptance as a *de facto* standard in notebook-size computers. It originated as a specification for add-on memory cards written by the Personal Computer Memory Card International Association.
peak to peak	a measure of signal amplitude; the difference between the highest and lowest excursions of the signal
PFI	Programmable Function Input
PGIA	Programmable Gain Instrumentation Amplifier
photoelectric sensor	an electrical device that responds to a change in the intensity of the light falling upon it
pipeline	a high-performance processor structure in which the completion of an instruction is broken into its elements so that several elements can be processed simultaneously from different instructions
PLC	programmable logic controller—a highly reliable special-purpose computer used in industrial monitoring and control applications. PLCs typically have proprietary programming and networking protocols, and special-purpose digital and analog I/O ports.
Plug and Play devices	devices that do not require DIP switches or jumpers to configure resources on the devices—also called switchless devices

Plug and Play ISA	a specification prepared by Microsoft, Intel, and other PC-related companies that will result in PCs with plug-in boards that can be fully configured in software, without jumpers or switches on the boards
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output
posttriggering	the technique used on a DAQ board to acquire a programmed number of samples after trigger conditions are met
potentiometer	an electrical device the resistance of which can be manually adjusted; used for manual adjustment of electrical circuits and as a transducer for linear or rotary position
ppm	parts per million
pretriggering	the technique used on a DAQ board to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition
propagation	the transmission of a signal through a computer system
propagation delay	the amount of time required for a signal to pass through a circuit
proportional control	a control action with an output that is to be proportional to the deviation of the controlled variable from a desired setpoint
protocol	the exact sequence of bits, characters, and control codes used to transfer data between computers and peripherals through a communications channel, such as the GPIB bus
proximity sensor	a device that detects the presence of an object without physical contact. Most proximity sensors provide a digital on/off relay or digital output signal.
pts	points
pulse trains	multiple pulses
pulsed output	a form of counter signal generation by which a pulse is outputted when a counter reaches a certain value

Q

quantization error	the inherent uncertainty in digitizing an analog value due to the finite resolution of the conversion process

R

referenced signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground. Also called grounded signal sources.
relative accuracy	a measure in LSB of the accuracy of an ADC. It includes all nonlinearity and quantization errors. It does not include offset and gain errors of the circuitry feeding the ADC.
resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244 percent of full scale.
retry	an acknowledge by a destination that signifies that the cycle did not complete and should be repeated
ribbon cable	a flat cable in which the conductors are side by side
rise time	the difference in time between the 10% and 90% points of a system’s step response
rms	root mean square
RSE	referenced single-ended mode
RTD	resistive temperature device
RTSI	Real-Time System Integration

S

s	seconds
S	samples

sample counter	the clock that counts the output of the channel clock, in other words, the number of samples taken. On boards with simultaneous sampling, this counter counts the output of the scan clock and hence the number of scans.
scan	one or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every analog input channel in the group.
SCANCLK	scan clock signal
scan clock	the clock controlling the time interval between scans. On boards with interval scanning support (for example, the AT-MIO-16F-5), this clock gates the channel clock on and off. On boards with simultaneous sampling (for example, the EISA-A2000), this clock clocks the track-and-hold circuitry.
scan rate	the number of scans per second. For example, a scan rate of 10 Hz means sampling each channel 10 times per second.
SCXI	Signal Conditioning eXtensions for Instrumentation
SE	single-ended inputs
self-calibrating	a property of a DAQ board that has an extremely stable onboard reference and calibrates its own A/D and D/A circuits without manual adjustments by the user
sensor	a device that responds to a physical stimulus (heat, light, sound, pressure, motion, flow, and so on), and produces a corresponding electrical signal
settling time	the amount of time required for a voltage to reach its final value within specified limits
S/H	sample-and-hold—a circuit that acquires and stores an analog voltage on a capacitor for a short period of time
signal conditioning	the manipulation of signals to prepare them for digitizing
signal divider	performing frequency division on an external signal
SISOURCE	SI counter clock signal
SMB	a type of miniature coaxial signal connector

SNR	signal-to-noise ratio—the ratio of the overall rms signal level to the rms noise level, expressed in decibels
software trigger	a programmed event that triggers an event such as data acquisition
software triggering	a method of triggering in which you simulate an analog trigger using software. Also called conditional retrieval.
source impedance	a parameter of signal sources that reflects current-driving ability of voltage sources (lower is better) and the voltage-driving ability of current sources (higher is better)
SOURCE input pin	an counter input pin where the counter counts the signal transitions
SS	simultaneous sampling—a property of a system in which each input or output channel is digitized or updated at the same instant
S/s	samples per second—used to express the rate at which a DAQ board samples an analog signal
STARTSCAN	start scan signal
STC	system timing controller
strain gauge	a thin conductor, which is attached to a material, that detects stress or vibrations in that material. The conductor’s resistance is a function of the applied force.
statically configured device	a device whose logical address cannot be set through software; that is, it is not dynamically configurable
successive-approximation ADC	an ADC that sequentially compares a series of binary-weighted values with an analog input to produce an output digital word in *n* steps, where *n* is the bit resolution of the ADC
switchless device	devices that do not require dip switches or jumpers to configure resources on the devices—also called Plug and Play devices
synchronous	(1) hardware—a property of an event that is synchronized to a reference clock (2) software—a property of a function that begins an operation and returns only when the operation is complete
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count
T/H	track-and-hold—a circuit that tracks an analog voltage and holds the value on command
THD	total harmonic distortion
THD+N	signal-to-THD plus noise—the ratio in decibels of the overall rms signal to the rms signal of harmonic distortion plus noise introduced
thermistor	a semiconductor sensor that exhibits a repeatable change in electrical resistance as a function of temperature. Most thermistors exhibit a negative temperature coefficient.
thermocouple	a temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
throughput rate	the data, measured in bytes/s, for a given continuous operation, calculated to include software overhead. Throughput Rate = Transfer Rate Software Overhead Factor
top-level VI	VI at the top of the VI hierarchy. This term is used to distinguish the VI from its subVIs.
transducer	See *sensor*
transducer excitation	a type of signal conditioning that uses external voltages and currents to excite the circuitry of a signal conditioning system into measuring physical phenomena
transfer rate	the rate, measured in bytes/s, at which data is moved from source to destination after software initialization and set up operations; the maximum rate at which the hardware can operate
TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
TTL	transistor-transistor logic

U

UART	universal asynchronous receiver/transmitter—an integrated circuit that converts parallel data to serial data (and vice versa), commonly used as a computer bus to serial device interface for serial communication
UI	update interval
UISOURCE	update interval counter clock signal
unipolar	a signal range that is always positive (for example, 0 to +10 V)
update	the output equivalent of a scan. One or more analog or digital output samples. Typically, the number of output samples in an update is equal to the number of channels in the output group. For example, one pulse from the update clock produces one update that sends one new sample to every analog output channel in the group.
UPDATE	update signal
update rate	the number of output updates per second
USB	Universal Serial Bus

V

V	volts
VDC	volts direct current
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{IN}	volts in
visual basic custom control (VBXs)	a specific form of binary packaged object that can be created by different companies and integrated into applications written using Visual Basic

V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage

W

waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal
wire	data path between nodes
word	the standard number of bits that a processor or memory manipulates at one time. Microprocessors typically use 8, 16, or 32-bit words.
working voltage	the highest voltage that should be applied to a product in normal use, normally well under the breakdown voltage for safety margin. See also *breakdown voltage*.

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