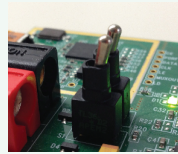# ADF4350 ADF4351

Cheat sheet

This document answers common questions relating to the usage of the ADF4350, ADF4351, and their evaluation boards.
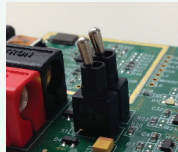
Evaluation Board

If only using one of the RFout SMA connectors, terminate the other with 50 Ω. This can be either a SMA termination or a 50 Ω resistor between the trace and GND.

To use USB power:

To use external power
(5.5 V on banana connectors):

Initialization Sequence

After powering up, write registers in this order:
    R5, R4, R3, R2, R1, R0

After initialization, to change output frequency, write registers in this order:
    [R4], [R1], R0
R4 only required if RF Divider changed.
R1 only required if MOD changed.

SPI Interface

If more than 32 bits are written to the SPI interface, the most recent 32 bits, on the rising edge of LE, are clocked into the ADF435x.

The maximum SPI CLK speed is 20 MHz.

When AV_{DD} is at 0 V, all SPI pins must be at 0 V.

Power Supplies

The V_{VCO} supply is very sensitive to noise. It is recommended to power V_{VCO} from a low noise supply.

All supply pins, including V_{VCO}, can share a supply.

Int-N Mode

Int-N mode is recommended if the fundamental VCO output frequency is an integer multiple of the PFD frequency; typically fixed frequency applications.

Setting FRAC = 0 (R1, DB[14:3]) automatically enables Int-N mode.

Verifying SPI Communication

Toggle DB5 (Powerdown) when programming R2 and check if current drawn changes.

Toggle DB6 (Phase Detector Polarity) when programming R2 and check if output signal frequency changes.

Program Muxout (R2, DB[28:26]) to its various states and monitor the Muxout pin.

Prescaler

ADF4350: if the input to the prescaler is >3 GHz, use 8/9 prescaler.
ADF4351: if the input to the prescaler is >3.6 GHz, use 8/9 prescaler.

Fundamental/Divided feedback (R4, DB23) will change the prescaler input frequency. For example, when the output frequency is 2195 MHz, the VCO fundamental output is actually 4390 MHz. If Fundamental feedback is used, 8/9 prescaler must be used. Alternatively, Divided feedback must be used so the prescaler input will be 2195 MHz.

When using 4/5 prescaler, the minimum N value is 23.
When using 8/9 prescaler, the minimum N value is 75.

Band Select and Settling Time

When R0 is written, the band select process selects the correct VCO band to output the desired frequency. Each band is approximately 46 MHz wide; so at the end of the band select process the output will be within 46 MHz of the desired output. Then, normal PLL settling occurs to lock the output to the desired output.
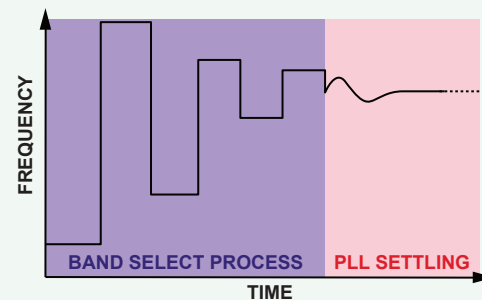
ADF4350: Band select process = 80 μs.
ADF4351: Band select process = 20 μs (if R3, DB23 is set to 1; otherwise, 80 μs. It is recommended to set DB23 to 1 unless the $f_{PFD} \leq$ 125 kHz).

PLL settling time is determined by the loop filter bandwidth and phase margin. Use ADIsimPLL to simulate loop dynamics.

Enabling Phase Adjust will disable the band select process. The output range will be limited to whatever band is currently is use (ADF4351 only).

PFD Frequency and Channel Spacing

The minimum channel spacing is set by:
$$f_{PFD} / MOD$$
where f_{PFD} = PFD frequency (maximum: 32 MHz in fractional-N mode);
MOD = R1, DB[14:3] = 2 to 4095.

Example: f_{PFD} = 32 MHz; MOD = 4095; channel spacing = 7.8 kHz.

Charge Pump Current

Increasing the charge pump current will increase the loop bandwidth. Decreasing it will decrease the loop bandwidth. ADIsimPLL™ shows the effect of changing the charge pump current.

It is recommended to design the loop filter at the middle charge pump current (2.5 mA), and then, after soldering the loop filter components, tweak the charge pump current to get the desired loop filter dynamic.

Phase Resync

When using phase resync, use Divided feedback (R4, DB23 = 0).

Set Clock Divider Value (R3, DB[14:3]) so that:
$$\frac{CLK\ Div \times MOD}{f_{PFD}} > PLL\ settling\ time$$

Phase Adjust (ADF4351 only)

When Phase Adjust (R1, DB28) is enabled, writing to R0 will increment the output phase by:
$$\frac{Phase\ Value\ (R1,\ DB[26:15])}{MOD\ (R1,\ DB[14:3])} \times 360°$$
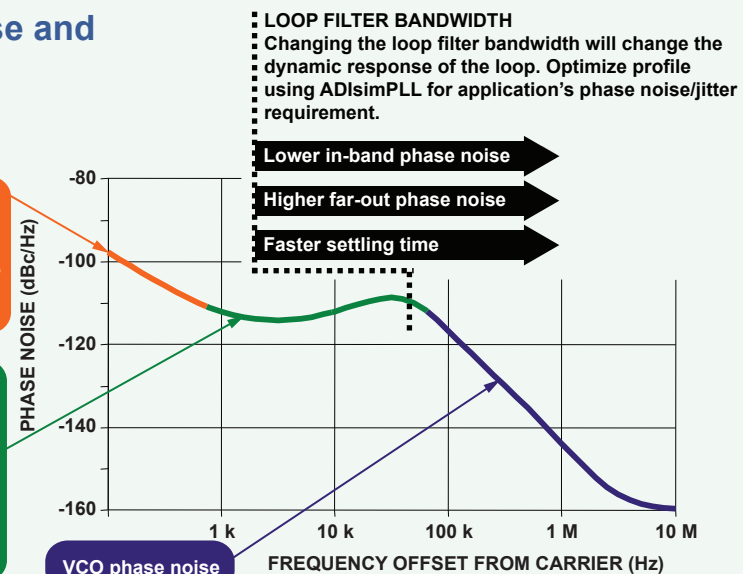relative to the current phase.

If FRAC = 0, R5 DB[18:15] must be set to 0b0100.

Do not use Phase Adjust and Phase Resync together.

Phase Noise and Loop Filter

Phase noise from the reference source. Reduce by using a lower phase noise reference source.

Phase noise from the phase detector, charge pump, and the loop filter. Reduce phase noise from phase detector and charge pump by maximizing PFD frequency.

VCO phase noise

LOOP FILTER BANDWIDTH
Changing the loop filter bandwidth will change the dynamic response of the loop. Optimize profile using ADIsimPLL for application's phase noise/jitter requirement.

Lower in-band phase noise
Higher far-out phase noise
Faster settling time

FRAC/MOD Reduction

When the FRAC/MOD fraction can be reduced, it is recommended to do so. Doing so will reduce fractional spurs by reducing the MOD value.

$$\frac{FRAC\ (R0,\ DB[14:3])}{MOD\ (R1,\ DB[14:3])} = \frac{25}{100}\ can\ be\ reduced\ to\ \frac{1}{4}$$

Use caution when using Phase Adjust or Low Spur Mode, as both use the MOD value.

This reduction is enabled by default in the evaluation board control software, but can be disabled in the Tools menu.
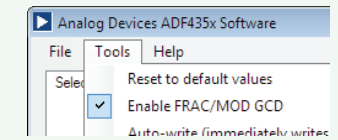
Muxout

Do not use *N counter to Muxout* setting during band select process (writing to R0). Enable *N counter to Muxout* after output has locked to new band.

RFout Relationship

RFoutA± is a differential signal; that is RFoutA− is 180° relative to RFoutA+.

RFoutB± is the same as RFoutA±, except delayed 80 ps, regardless of frequency.

Output Frequency Error

Any offset in the reference source will be multiplied by N, and appear as an offset at the output.

Register settings may be incorrect. Use evaluation board control software to generate register values.

Powerdown

Hardware powerdown (CE pin) or software powerdown (R2, DB5) will retain register contents.

Powering down the AV_{DD} and DV_{DD} pins will lose register contents.

Low Spur Mode

When using Low Spur Mode, MOD must be 50 or greater.

Support

For further support, follow the EngineerZone® link below.

v0.12 - September 2014

ANALOG DEVICES