# MAX 10 Power Management User Guide

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UG-M10PWR
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# MAX 10 Power Management Overview

# 1

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MAX® 10 devices offer the following power supply device options:

- Single-supply device—requires 1 external power supply of 3.0 V or 3.3 V while offering maximum convenience and board simplicity.
- Dual-supply device—requires 2 external power supplies of 1.2 V and 2.5 V while offering the most features, highest performance, and when coupled with high-efficiency Enpirion® PowerSoCs, the lowest power solution.

**Related Information**

MAX 10 Power Management Features and Architecture on page 2-1
Provides information about power management features and architecture



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# MAX 10 Power Management Features and Architecture

# 2

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MAX 10 power optimization features are as follows:

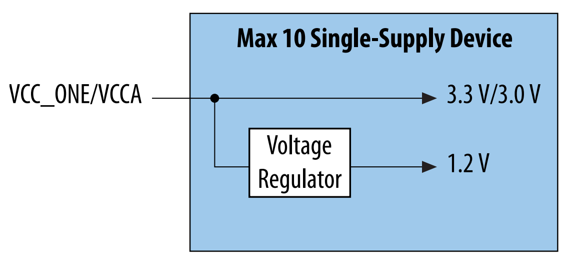
- Single-supply or dual-supply device options
- Power-on reset (POR) circuitry
- Power management controller scheme
- Hot socketing

## Power Supply Device Options

### Single-Supply Device

MAX 10 single-supply devices only need either a 3.0- or 3.3-V external power supply. The external power supply serves as an input to the MAX 10 device `VCC_ONE` and `VCCA` power pins. This external power supply is then regulated by an internal voltage regulator in the MAX 10 single-supply device to 1.2 V. The 1.2-V voltage level is required by core logic operation.

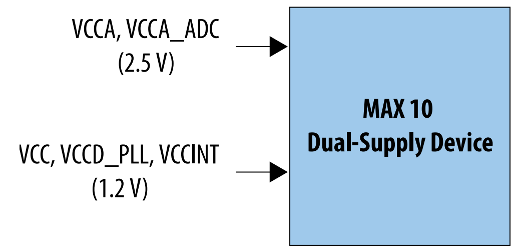
**Figure 2-1: MAX 10 Single-Supply Device**




### Dual-Supply Device

MAX 10 dual-supply devices require 1.2 V and 2.5 V for the device core logics and periphery operations.

**Figure 2-2: MAX 10 Dual-Supply Device**




## Comparison of the MAX 10 Power Supply Device Options

### Table 2-1: Comparison of the MAX 10 Power Supply Device Options

| Characteristics | Single-Supply Device | Dual-Supply Device |
|---|---|---|
| Voltage regulator count (1) | 1 | 2 |
| Core and I/O performance | Low | High |

For MAX 10 single-supply devices, only one power supply is required—3.0 V or 3.3 V to power the core of the FPGA. The same power supply can be used to power the I/O if the same 3.0 V or 3.3 V voltage is required. If different I/O voltage is used, then additional voltage regulators will be needed.

For MAX 10 dual-supply devices, two power supplies are required to supply power to the device core, periphery, phase-locked loop (PLL), and analog-to-digital converters (ADC) blocks—1.2 V and 2.5 V. Depending on the I/O standard voltage requirement, you may use two or more voltage regulators.

As the power rails for the FPGA core are supplied externally in the MAX 10 dual-supply devices, the design can be optimized for power by using high efficiency switching power supplies on the board. The power savings will be equal to the increased efficiency of the regulators used compared to the internal linear regulators of the MAX 10 single-supply devices. If linear regulators are used to power the MAX 10 dual-supply devices, the power consumption of the MAX 10 dual-supply devices will be approximately equal to the MAX 10 single-supply devices.

The device performance of the single-supply device is lower than that of the dual-supply device. For the performance difference in terms of LVDS, pseudo-LVDS, digital signal processing (DSP), and internal memory performance, refer to the MAX 10 FPGA device datasheet.

**Related Information**

**MAX 10 FPGA Device Datasheet**
Provides details about the MAX 10 performance difference in terms of LVDS, pseudo-LVDS, DSP, and internal memory performance.

(1) This shows the number of power supplies required by the core and periphery of the MAX 10 devices. You may need additional voltage regulators to supply power to the `VCCIO` if the `VCCIO` does not have the same voltage level as the core and periphery supply.

## Power Supply Design

Designing a power tree for a MAX 10 single- or dual-supply device will vary depending on the static and dynamic power, as well as I/O and other feature utilization, for each specific use case.

The Altera® Enpirion portfolio of power management solutions, combined with comprehensive design tools, enable optimized MAX 10 device power supply design. The Enpirion portfolio includes power management solutions that are compatible with all MAX 10 variants.

The *MAX 10 FPGA Device Family Pin Connection Guidelines* provides a more detailed recommendation about how to group inputs to power a MAX 10 device. The PowerPlay Early Power Estimators (EPE) tool for MAX 10 devices provides input rail power requirements and specific device recommendations based on each specific MAX 10 use case.

Individual input rail voltage and current requirements are summarized on the **Report** tab while input rail groupings and specific power supply recommendations can be found on the **Main** and **Enpirion** tabs, respectively.

**Warning:** MAX 10 single-supply devices have maximum power consumption of $V_{CC\_ONE}$, as listed in the following table. Running a design that goes beyond the maximum power consumption of $V_{CC\_ONE}$ of the MAX 10 single-supply device may cause functional issue on the device. Therefore, ensure that your device does not exceed the maximum power consumption of $V_{CC\_ONE}$ when you analyze the power consumption of your design using the PowerPlay EPE spreadsheet.

**Table 2-2: Maximum Power Consumption of $V_{CC\_ONE}$ for MAX 10 Single-Supply Devices**

| Device | Maximum Power Consumption (W) |
|---|---|
| 10M02S | 0.778 |
| 10M04S | 1.362 |
| 10M08S | 1.362 |
| 10M16S | 2.270 |
| 10M25S | 2.943 |
| 10M40S | 5.267 |
| 10M50S | 5.267 |

**Related Information**

- **Enpirion Power Management Solutions**
  Provides more information about Altera's Power Management IC and PowerSoC solutions designed for powering FPGAs.
- **MAX 10 FPGA Device Family Pin Connection Guidelines**
  Provides a more detailed recommendation about how to group inputs in order to power a MAX 10 device.

### Transient Current

You may observe a transient current at the $V_{CCIO}$ power supply when powering up the MAX 10 devices. The transient current of $V_{CCIO}$ applies to all $V_{CCIO}$ voltage levels supported by the MAX 10 device.

**Table 2-3: Maximum $V_{CCIO}$ Power Supply Transient Current for MAX 10 Devices**

| Device | Maximum Power Supply Transient Current (mA) | Duration (s) |
|---|---|---|
| 10M02 | 220 | 25% of the ramp time |
| 10M04 | 290 | |
| 10M08 | 300 | |
| 10M16 | 430 | |
| 10M25 | 510 | |
| 10M40 | 670 | |
| 10M50 | 680 | |

**Note:** The value of the transient current is based on the zero decoupling capacitance on the characterization board. The observed value will be less than the published value after adding the decoupling capacitance on your design board. Altera recommends using a soft start regulator that is able to reduce the transient current when the device is powered.

## Power-On Reset Circuitry

The POR circuitry keeps the MAX 10 device in the reset state until the POR monitored power supply outputs are within the recommended operating range of the maximum power supply ramp time, $t_{RAMP}$.

If the ramp time, $t_{RAMP}$, is not met, the MAX 10 device I/O pins and programming registers remain tri-stated, during which device configuration could fail.

The MAX 10 device POR circuit monitors the following power rails during power up regardless of the power supply device options:

- $V_{CC}$ or regulated $V_{CC\_ONE}$
- $V_{CCIO}$ of banks 1B and 8 [(2)]
- $V_{CCA}$

The POR circuitry also ensures $V_{CCIO}$ level of I/O banks 1B and 8[(2)] that contain configuration pins reach an acceptable level before configuration is triggered.

(2) $V_{CCIO}$ of banks 1 and 8 for the 10M02 device.

# Power Supplies Monitored and Not Monitored by the POR Circuitry

### Table 2-4: Power Supplies Monitored and Not Monitored by the POR Circuitry

| Power Supply Device Options | Power Supplies Monitored | Power Supplies Not Monitored |
|---|---|---|
| Single-supply device | • Regulated $V_{CC\_ONE}$<br>• $V_{CCA}$<br>• $V_{CCIO}$ (3) | — |
| Dual-supply device | • $V_{CC}$<br>• $V_{CCA}$<br>• $V_{CCIO}$(3) | • $V_{CCD\_PLL}$<br>• $V_{CCA\_ADC}$<br>• $V_{CCINT}$ |

The MAX 10 POR circuitry uses an individual POR-detecting circuitry to monitor each of the configuration-related power supplies independently. The outputs of all the individual POR detectors gate the main POR circuitry. The main POR circuitry waits for all individual POR circuitries to release the POR signal before allowing the control block to start programming the device. The main POR is released after the last ramp-up power reaches the POR trip level followed by a POR delay.

By default, the Quartus® Prime software assigns POR delay time to standard POR delay. For applications that need fast wake-up to begin operation, you can enable fast POR delay time on the Quartus Prime programmer user interface.

(3) For banks 1B and 8 for all MAX 10 devices and banks 1 and 8 for the 10M02 device.

**Figure 2-3: Relationship Between $t_{RAMP}$ and POR Delay**

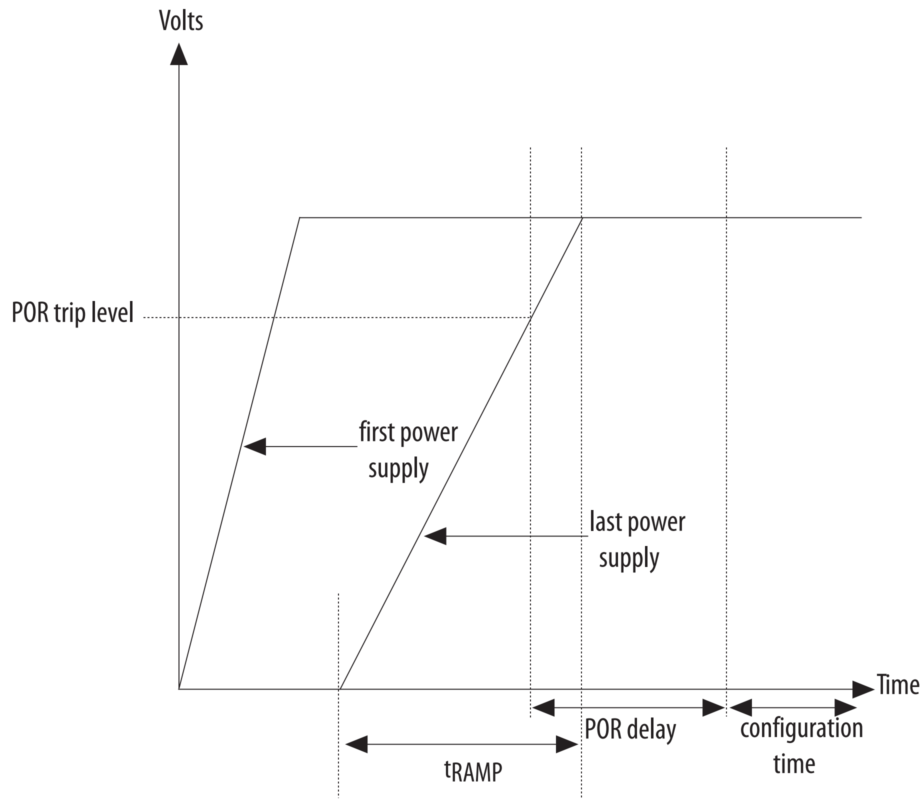
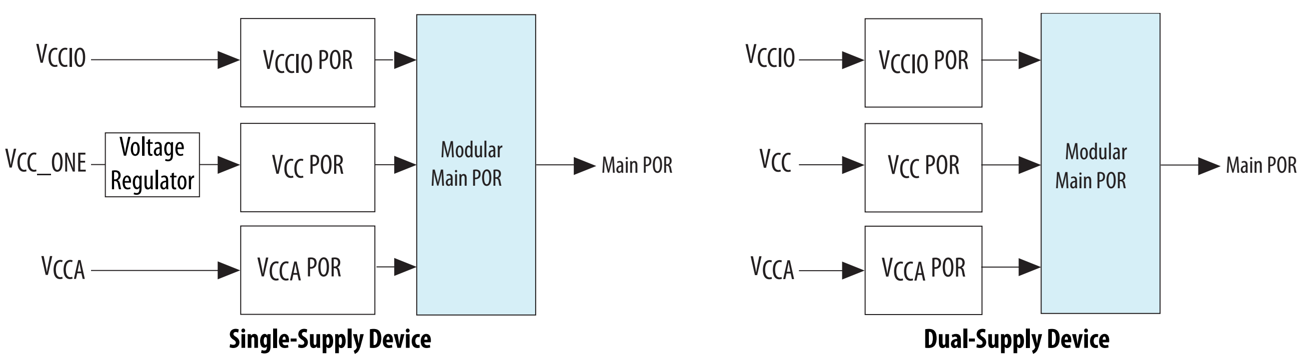



**Figure 2-4: Simplified POR Diagram for MAX 10 Devices**




After the MAX 10 device enters user mode, the POR circuit continues to monitor the $V_{CCA}$ and $V_{CC}$ power supplies. This is to detect a brown-out condition during user mode. If either the $V_{CCA}$ or $V_{CC}$ voltages go below the POR trip point during user mode, the main POR signal is asserted. When the main POR signal is asserted, the device is forced into reset state. $V_{CCIO}$(3) is monitored by the POR circuitry. In the event of the $V_{CCIO}$(3) voltage drops during user mode, the POR circuit does not reset the device. However, if you are using instant-on features, the POR circuit does monitor the VCCIO voltage drop for up to 9 ms after the last power rail reaches its trip point.

## Instant-On Support

In some applications, it is necessary for a device to wake up very quickly to begin operation. The MAX 10 device offers the instant-on feature to support fast wake-up time applications. With the instant-on feature, MAX 10 devices can directly enter configuration mode without any POR delay after the POR trips for the monitored power supplies. Then your design can be configured from internal configuration flash memory (CFM). This feature provides the shortest time to enter user mode as a whole.

To benefit from the instant-on feature of the MAX 10 device, there is a power-up sequence and ramp time requirement to follow. The following table shows the power-up sequence requirement for different power supply device options. For the minimum and maximum ramp time, refer to the recommended operating conditions in the *MAX 10 FPGA Device Datasheet*.

### Instant-On Requirement

**Table 2-5: Instant-On Power-Up Sequence Requirement**

| Power Supply Device Options | Power-Up Sequence |
|---|---|
| Single-supply device | $V_{CCIO}$ must ramp up to full rail before $V_{CCA}$ and $V_{CC\_ONE}$ start ramping. |
| Dual-supply device | All power supplies must ramp up to full rail before $V_{CC}$ starts ramping. |

**Related Information**

**MAX 10 FPGA Device Datasheet**

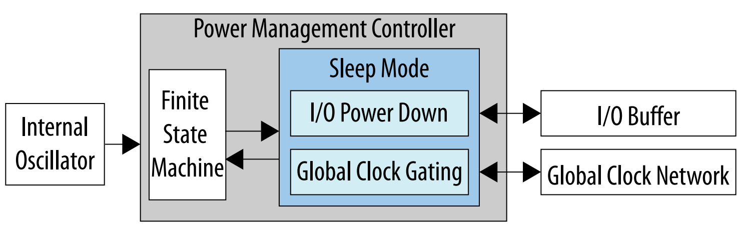
Provides details about the MAX 10 ramp time requirements, internal oscillator clock frequency, and hot-socketing specifications.

## Power Management Controller Scheme

The power management controller scheme allows you to allocate some applications in sleep mode during runtime. This enables you to to turn off portions of the design, thus reducing dynamic power consumption. You can re-enable your application with a fast wake-up time of less than 1 ms.

## Power Management Controller Architecture

**Figure 2-5: Power Management Controller Architecture**




The MAX 10 device contains hardware features that enable I/O power down and global clock (GCLK) gating to manage low-power state during sleep mode. You can power down the I/O buffer dynamically when your application is in idle or sleep mode. One example is the digital single lens reflex DSLR camera application where the LVDS I/O needs to be powered down during the idle condition. Without touching any buttons, the screen turns off while the camera is still powered on.

Altera provides a soft power management controller as reference design utilizing low-power features implemented in the MAX 10 devices. You can modify the reference design based on your application. The soft power management controller includes a simple finite state machine (FSM) to manage the low-power state mode by powering down the I/O buffer and GCLK gating during sleep mode.

All MAX 10 devices contain hardware features for clock gating. The 10M16, 10M25, 10M40, and 10M50 devices contain hardware features for I/O power down. With hardware features, you can manage the low-power state during sleep mode by using the soft power management controller that you define.

You can implement the power management controller in FPGA core fabric with a minimum of one I/O port reserved for sleep mode enter and exit signals.

## Internal Oscillator

The internal oscillator clocks the power management controller operation. The internal oscillator is routed from flash to the core. The internal oscillator enables the power management controller to detect the wake-up event and the sleep mode event. In order to enable the internal oscillator clock when the power management controller is enabled, you have to set `oscena` to `1`. For the clock frequency of the internal oscillator, refer to the *MAX 10 FPGA Device Datasheet*.

**Related Information**

**MAX 10 FPGA Device Datasheet**
Provides details about the MAX 10 ramp time requirements, internal oscillator clock frequency, and hot-socketing specifications.

## I/O Buffer Power Down

The MAX 10 device has a dynamic power-down feature on some of the I/O buffers that have high-static power consumption. The dynamic power-down feature is only applicable for the I/O buffers that have been programmed for the I/O standards in the following table.

**Table 2-6: I/O Buffer Power Down**

| I/O Buffer | I/O Standards | Control Port | Control Signal Capability |
|---|---|---|---|
| Input | SSTL, HSTL, HSUL, and LVDS | `nsleep` | 1 per I/O bank[4] |
| Output | All I/O standards | `oe` | 1 per I/O buffer |

During power-up and configuration modes, the soft power management controller is not yet configured and the control signals are forced to `1` (inactive). After configuration mode, when the power management controller is activated, the power management controller will default the control signals to `1`. When control signals are `0`, the power management controller powers down or tri-states the I/O buffers. Subsequently the I/O is put into the sleep mode.

The MAX 10 device I/O buffers need to maintain the previous states during the sleep mode operation. The previous states in your core logics remain upon exiting the sleep mode.

(4) I/O banks 1A and 1B share one control signal.

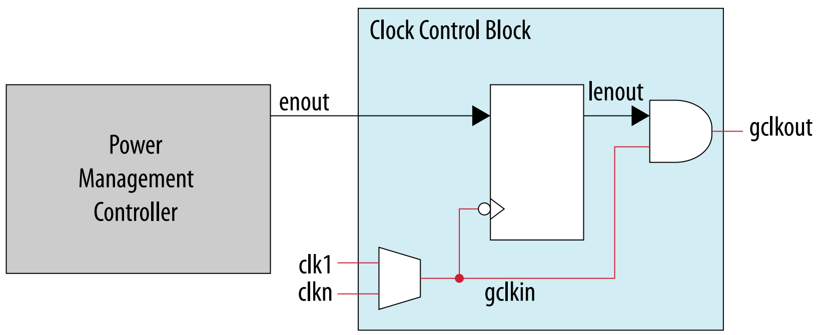
## Global Clock Gating

The dynamic power-down feature is available in GCLK networks only. You can use the power management controller for the dynamic power-down of a GCLK network by controlling the active high `enout` signal. The GCLK networks serve as low-skew clock sources for functional blocks such as logic array blocks (LABs), DSP, embedded memory, and PLLs.

When a GCLK network is gated, all the logics fed by the GCLK network are in off-state. This reduces the overall power consumption of the device. The dynamic power-down feature allows core logics to control the following power-up and power-down conditions of the GCLK networks:

- Power down synchronously or asynchronously
- Power up asynchronously

**Figure 2-6: GCLK Gating**




# Hot Socketing

The MAX 10 device offers hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove the MAX 10 device on a board in a system during system operation. This does not affect the running system bus or the board that is inserted into the system.

The hot-socketing feature removes some encountered difficulties when using the MAX 10 device on a PCB that contains a mixture of devices with different voltage levels.

With the MAX 10 device hot-socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board. MAX 10 device hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

## Hot-Socketing Specifications

The MAX 10 device is a hot-socketing compliant device that does not need any external components or special design requirements. Hot-socketing support in the MAX 10 device has the following advantages:

- You can drive the devices before power up without damaging the device.
- I/O pins remain tri-stated during power up. The device does not drive out before or during power up, therefore not affecting other buses in operation.

### Drive MAX 10 Devices Before Power Up

Before or during power up or power down, you can drive signals into I/O pins, dedicated input pins, and dedicated clock pins without damaging the MAX 10 devices.

The MAX 10 device supports any power-up or power-down sequence to simplify system-level design.

### I/O Pins Remain Tri-stated During Power up

The output buffers of the MAX 10 device are turned off during system power up or power down. The MAX 10 device family does not drive out until the device is configured and working in recommended operating conditions. The I/O pins are tri-stated until the device enters user mode with a weak pull-up resistor to $V_{CCIO}$.

A possible concern for semiconductor devices in general regarding hot-socketing is the potential for latch up. Latch up can occur when electrical subsystems are hot-socketed into an active system. During hot-socketing, the signal pins may be connected and driven by the active system. This occurs before the power supply can provide current to the $V_{CC}$ of the device and ground planes. This condition can lead to latch up and cause a low-impedance path from $V_{CC}$ to ground in the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

The design of the I/O buffers and hot-socketing circuitry ensures that the MAX 10 device family is immune to latch up during hot-socketing.

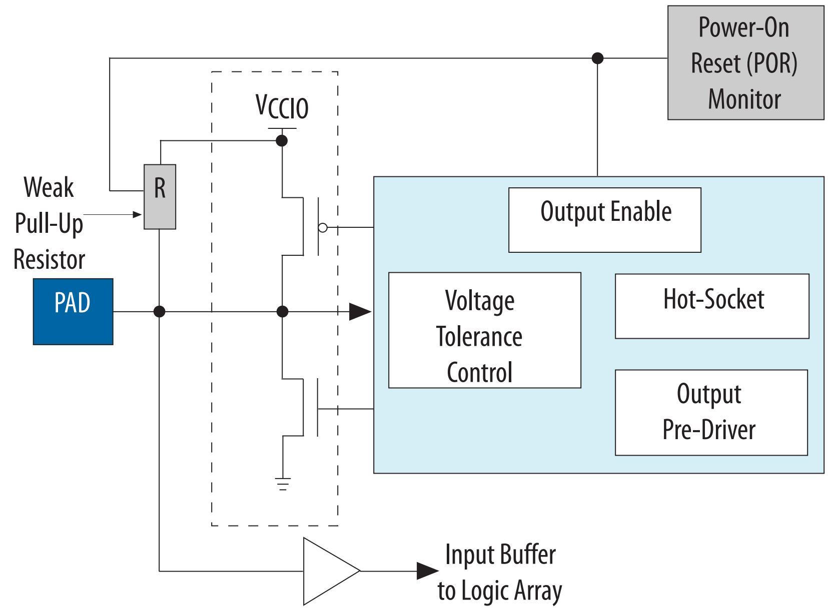
**Related Information**

**MAX 10 FPGA Device Datasheet**
Provides details about the MAX 10 ramp time requirements, internal oscillator clock frequency, and hot-socketing specifications.

## Hot-Socketing Feature Implementation

The hot-socketing feature tri-states the output buffer during the power-up ($V_{CCIO}$ or $V_{CC}$ power supplies) or power-down event. The hot-socketing circuitry generates an internal `HOTSCKT` signal when $V_{CCIO}$ or $V_{CC}$ is below the threshold voltage during power up or power down. The `HOTSCKT` signal cuts off the output buffer to ensure that no DC current leaks through the pin (except for weak pull-up leaking). Each I/O pin has the circuitry shown in the following figure. The hot-socketing circuit does not include `CONF_DONE` and `nSTATUS` pins to ensure that these pins are able to operate during configuration. Thus, it is an expected behavior for these pins to drive out during power-up and power-down sequences.

**Figure 2-7: Hot-Socketing Circuitry for MAX 10 Devices**




The POR circuit monitors the voltage level of power supplies and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor in MAX 10 device I/O elements (IOE) keeps the I/O pins from floating. The voltage tolerance control circuit protects the I/O pins from being driven before $V_{CCIO}$ and $V_{CC}$ supplies are powered up. This prevents the I/O pins from driving out when the device is not in user mode.

Altera uses GND as reference for hot-socketing operation and I/O buffer designs. To ensure proper operation, Altera recommends connecting the GND between boards before connecting the power supplies. This prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND can cause an out-of-specification I/O voltage or current condition with the Altera device.

# Power Management Controller Reference Design 3

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This reference design utilizes the low-power feature supported in MAX 10 devices. The following figure shows the related block diagrams in the power management controller reference design.

**Figure 3-1: Power Management Controller Block Diagram**

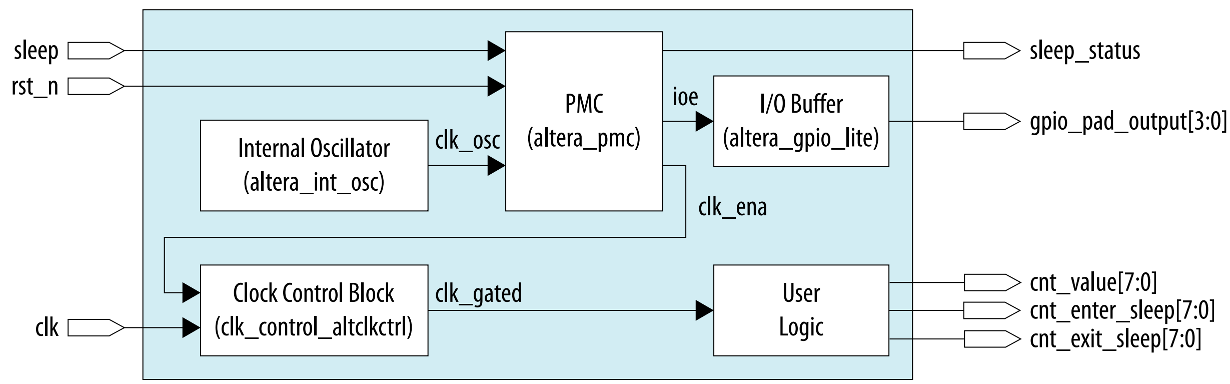



**Table 3-1: Input and Output Ports of the Power Management Controller Reference Design**

| Port Name | Input/Output | Description |
|---|---|---|
| `sleep` | Input | Sleep control. |
| `rst_n` | Input | Active low reset signal. |
| `clk` | Input | Clock signal. |
| `sleep_status` | Output | Sleep status of the system. This signal is asserted high when the system is entering the sleep mode condition. This signal is de-asserted when the system exits the sleep mode condition completely. |
| `gpio_pad_output[3:0]` | Output | General-purpose I/O (GPIO) output ports. |
| `cnt_value[7:0]` | Output | Free-running counter value in user logic. |
| `cnt_enter_sleep[7:0]` | Output | Counter value when the system is entering sleep mode condition. |

| Port Name | Input/Output | Description |
|---|---|---|
| `cnt_exit_sleep[7:0]` | Output | Counter value when the system is exiting sleep mode condition. |

The power management controller design is a FSM showing the state of powering down and powering up global clocks (GCLKs) and I/O buffers. The internal oscillator, clock control block, and I/O buffer are intellectual property (IP) that are supported by the Quartus Prime software and you can instantiate the IPs from the IP catalog. The user logic can be any logical circuitry that are implemented using logic element (LE) and an embedded component such as DSP and internal memory in your design. In this reference design, the user logic used is a free-running 8-bit counter. The `cnt_enter_sleep` and `cnt_exit_sleep` ports are used to ensure user logic can enter and exit sleep mode without data corruption. It is expected for that `cnt_enter_sleep[7:0]` and `cnt_exit_sleep[7:0]` are at the same value after the user logic enter and exit sleep mode. `gpio_pad_output` ports demonstrate tri-stated state of the GPIO when the system is in sleep mode.

**Related Information**

PMC Reference Design

## Clock Control Block

The clock control IP core (`clk_control_altclkctrl`) is an IP provided in the Quartus Prime software. This IP is used to control the clock system in the device. The GCLKs that drive through the device can be dynamically powered down by controlling the active high `ena` signal. The `ena` port is an input to the clock control IP block. When this IP is instantiated, select the `ena` port to enable the controls of GCLKs.

## I/O Buffer

Altera GPIO Lite IP core (`altera_gpio_lite`) is implemented as an input, output, or bidirectional I/O buffer. You can control the power down of these I/O buffers by enabling the `nsleep` port of the input buffer and the `oe` port of the output buffer. The `oe` and `nsleep` ports are pulled low by the power management controller design to power down the I/O buffers during sleep mode. Altera recommends using a separate Altera GPIO Lite IP when some of the I/O buffer is not required to be powered down.

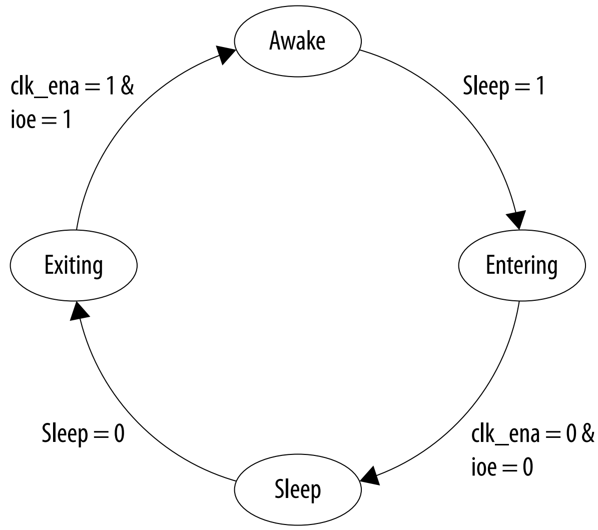
## Internal Oscillator

Internal Oscillator IP core (`altera_in_osc`) is a free-running oscillator once you enable it. This oscillator runs throughout the entire power management controller design.

## Power Management Controller

The power management controller implements a simple FSM to control the power-up and power-down sequences of the GCLK networks and I/O buffer.

**Figure 3-2: FSM of the Power Management Controller**




## Entering State

When the power management controller detects a sleep event, the FSM transitions to the Entering state and performs power-down operation on I/O buffers and GCLK networks. A sleep event is detected when the `sleep` signal is asserted. A sleep event could be triggered by an internal or external request.

## Sleep State

After the power-down operation on I/O buffers and GCLK networks, the FSM transitions to the Sleep state and waits for the wake-up event. This state is the sleep mode state.

## Exiting State

When the power management controller detects a wake-up event, the FSM transitions to the Exiting state and performs power-up operation on I/O buffers and GCLK networks. A wake-up event is detected when the `sleep` signal is de-asserted. A wake-up event could be triggered by an internal or external request such as interruption or time-out on some counters..

## Awake State

After the power-up operation on I/O buffers and GCLK networks, the FSM transitions to the Awake state.

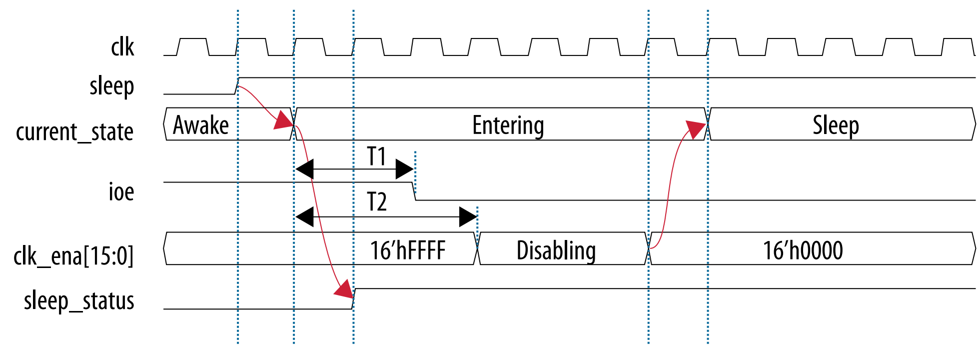
This process repeats when a sleep event is initiated again.

# Entering or Exiting Sleep Mode

During power-up and configuration modes, the `sleep` signal must be low. When the `sleep` signal is asserted, the device immediately enters sleep mode. Upon entering sleep mode, the functionality of the device such as GCLK networks and I/O buffers are dynamically powered down—to minimize dynamic power dissipation. All configuration data is retained when the device is in the sleep mode.

## Entering Sleep Mode

**Figure 3-3: Entering Sleep Mode Timing Diagram**

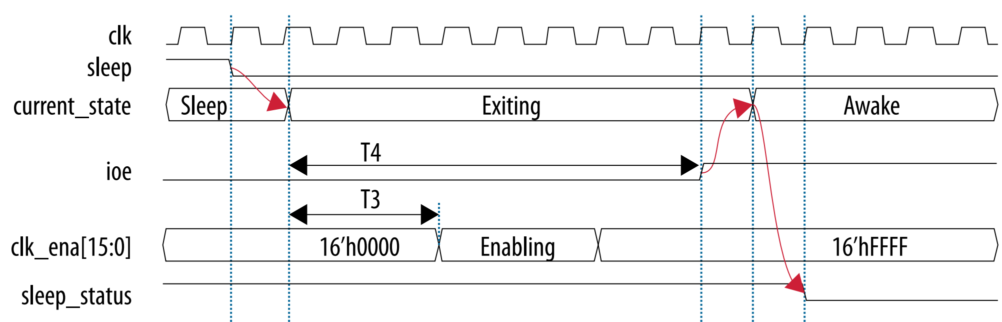



The following sequence occurs when the device enters sleep mode:

1. An internal or external request drives the `sleep` signal high, forcing the device to go into sleep mode.
2. After a delay of T1, the power management controller powers down all the I/O buffers by de-asserting `ioe` signal that connects to `oe` and `nsleep` ports of the I/O buffers.
3. After a delay of T2, the power management controller turns off all GCLK networks by disabling `clk_ena[15:0]` signal from LSB to MSB. After three clock cycles, the `clk_ena[15:0]` signal is fully disabled and transits into the sleep state.
4. The power management controller remains in sleep state until the `sleep` signal is de-asserted.
5. User logic will latch the running counter value before entering the sleep state and output to `cnt_sleep_enter` port. The running counter is then frozen.
6. `gpio_pad_output` (GPIO) is tri-stated when `ioe` is de-asserted.

## Exiting Sleep Mode

**Figure 3-4: Exiting Sleep Mode Timing Diagram**



The following sequence occurs when the device exits sleep mode:

1. An internal or external request drives the `sleep` signal low, forcing the device to exit sleep mode.
2. After a delay of T3, the power management controller turns on all GCLK networks by enabling `clk_ena[15:0]` signal from LSB to MSB. After three clock cycles, the `clk_ena[15:0]` signal is fully enabled and all GCLK networks are turned on.
3. After a delay of T4, the power management controller powers up all the I/O buffers by asserting the `ioe` signal.
4. The power management controller remains in awake state until the `sleep` signal is asserted.
5. User logic will latch the running counter value before the awake state and output to `cnt_sleep_exit` port. The running counter is then release from freeze.
6. `gpio_pad_output` (GPIO) is driving its output value when `ioe` is asserted.

## Timing Parameters

The following table lists the definition and minimum value of the T1, T2, T3, and T4 parameters in the entering sleep mode timing diagram and exiting sleep mode timing diagram, respectively.

**Table 3-2: T1, T2, T3, and T4 Parameters Minimum Value and Definition**

| Parameter | Width (bits) | Minimum Value (Decimal) | Description |
|---|---|---|---|
| T1 | 6 | 1 | `ioe` disable timing. |
| T2 | 6 | 11 | `clk_ena` disable timing. |
| T3 | 6 | 1 | `clk_ena` enable timing. |
| T4 | 6 | 40 | `ioe` enable timing. |

T1, T2, T3, and T4 can be increased based on your system requirement.

# Hardware Implementation and Current Measurement

This design is implemented using the 10M50DAF484C8 device. You can implement this design using any MAX 10 device. This design runs on the MAX 10 Development Kit Board to show current and power relative between user mode and sleep mode.

The resource utilization of this design is as follows:

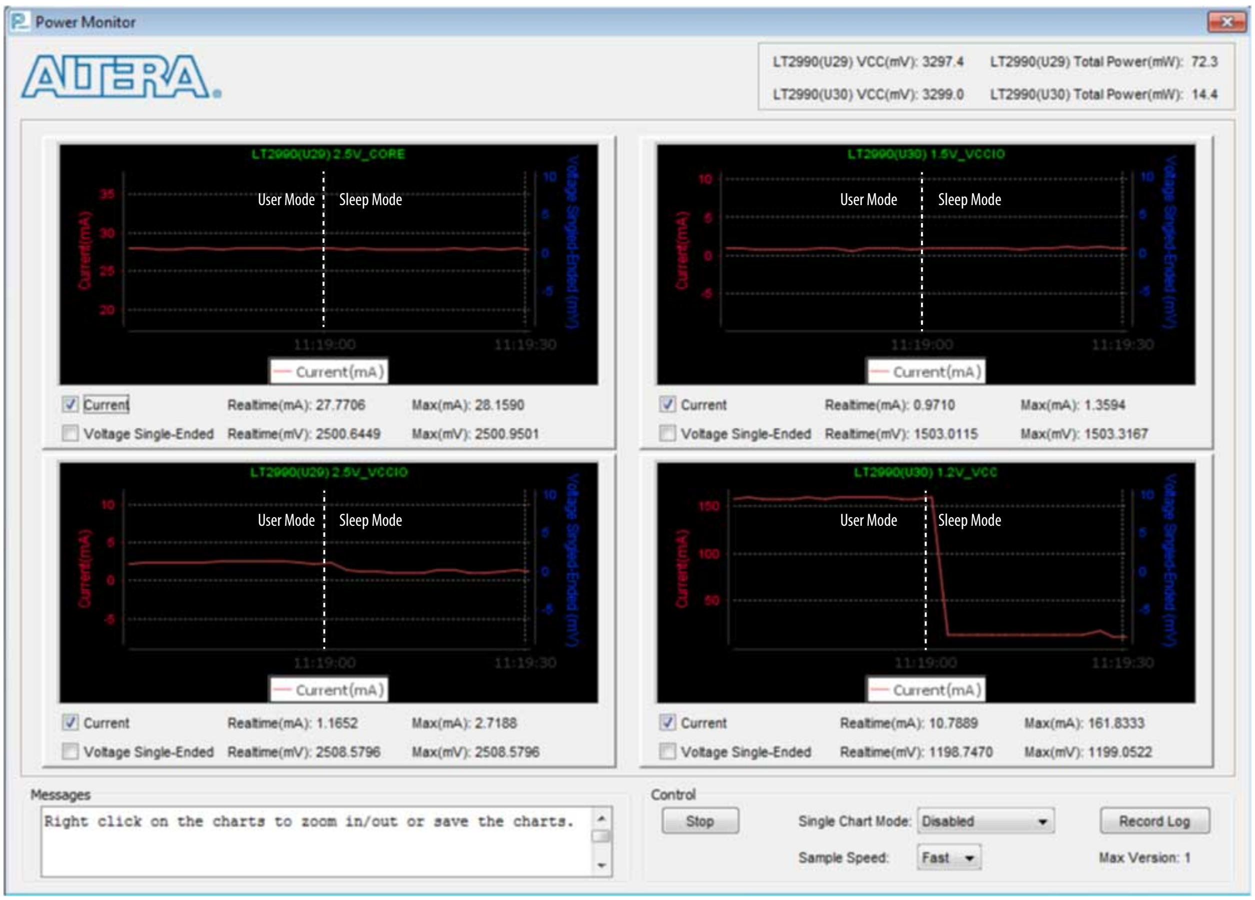
- 42,000 LEs (84% of total LEs)—gray counter top module utilizes most of the LEs in the device
- 33 I/O pins (9% of total pins)—covering 3 input pins and 30 output pins

The current in this design is measured using a current monitor component (the Linear Technologies LTC 2990). The measured current is further processed by a pre-programmed design in a MAX II device. The measured current is shown on Altera power monitor GUI when the PowerMonitor.exe is launched. You will see a current monitor for each of the main supplies to the MAX 10 device as follows:

- 2.5V_CORE[5]
- 2.5V_VCCIO
- 1.5V_VCCIO
- 1.2V_VCC

For design demonstration purpose, the push button is used for sleep control and the LEDs are used for sleep status. Thus, these signals have been inverted on the pin level. To enter sleep mode, press and hold the push button USER_PB0. To release the design to user mode, release the push button USER_PB0. LED0 indicates the sleep status of the device. LED0 is turned on when the device enters sleep mode and is turned off when the device is in user mode. During sleep mode, `gpio_pad_output` ports connecting to LED1–LED4 are tri-stated and then turned off.

**Figure 3-5: Current Monitor for Each Supply**




In sleep mode, all GCLK networks are gated and all output buffers are disabled.

(5) This is 2.5V_VCCA.

**Table 3-3: Comparison of Current and Power Consumption**

| Current and Power | User Mode | Sleep Mode |
|---|---|---|
| 1.2V_ICC (mA) | 160 | 11 |
| 2.5V_ICCA (mA) | 28 | 28 |
| 1.5V_ICCIO (mA) | 1.3 | 1.0 |
| 2.5V_ICCIO (mA) | 2.7 | 1.2 |
| Total power (mW) | 270 | 88 |

The results show an approximate 93% reduction in the core current (1.2V_ICC) consumption and an approximate 56% reduction in I/O current (2.5V_ICCIO) consumption in sleep mode relative to user mode. The total power consumption reduction in this design in sleep mode is about 68%.

# Additional Information for MAX 10 Power Management User Guide

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2015.11.02

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## Document Revision History for MAX 10 Power Management User Guide

| Date | Version | Changes |
|---|---|---|
| November 2015 | 2015.11.02 | • Added the Transient Current section.<br>• Changed instances of Quartus II to Quartus Prime. |
| February 2015 | 2015.02.09 | Added the MAX 10 Power Management Controller Reference Design. |
| December 2014 | 2014.12.15 | • Updated the MAX 10 Power Management Overview section.<br>• Updated the Dual-Supply Device section to update details on power consumption for dual-supply devices.<br>• Updated the Power Supply Design section to include the maximum power consumption for each MAX 10 single-supply device.<br>• Updated the Power Management Controller Scheme section to include updates on sleep mode. |
| September 2014 | 2014.09.22 | Initial release. |