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Light localization for broadband integrated optics in three dimensions

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We demonstrate a universal mechanism for high-bandwidth, lossless, subwavelength scale circuitry in a fully three-dimensional (3D) all-optical microchip. Here light is confined and guided in air by wave interference, rather than total internal reflection. Our 3D circuit design consists of several planar microchip layers linked by vertical waveguides. The 3D microchip enables up to 200 nm single-mode waveguiding in each planar chip layer and 100 nm bandwidth chip-to-chip interconnects in a variety of 3D photonic band gap materials.

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Dense integration of information-processing components into a small volume is a major goal of the fields of nanoelectronics, plasmonics, and photonics. Electronic microchips are inherently single-channel device arrays placed within a two-dimensional circuit board. Heat dissipation, cross talk between circuit elements, and manufacturing cost are critical issues in the effort to miniaturize electronic circuits toward the nanometer scale. In contrast, photonics enables multiple wavelength channels of simultaneous information flow without cross talk or heat dissipation problems. The central challenge in ultradense integrated optics for information processing lies in the fundamental difficulty to confine light by conventional means on subwavelength scales without prohibitive diffractive spread, scattering, and radiation losses. In this paper, these fundamental problems are circumvented in certain dielectric microstructures using the principle of light localization.

Light localization[1,2] is a fundamental optical phenomenon arising from strong resonant scattering and interference effects.[3] In the context of photonic band gap (PBG) materials,[2,4,5] localization of light arises from destructive wave interference in all spatial directions resulting from carefully engineered scattering resonances. Unlike total internal reflection in a conventional high-refractive-index microcavity, light localization enables confinement in a low-index medium such as air. For example, two-dimensional (2D) light localization enables confinement and guiding of light along the air core of certain photonic crystal fibers.[6,7] Three-dimensional (3D) light localization by single defects in three-dimensional PBG materials facilitates optical microcavities with almost arbitrarily high quality (Q) factors with subwavelength scale mode volumes.[8] Light localization based waveguiding in photonic crystals[5,9–15] allow complete confinement of light even at sharp bends.[9–11,15] Here, we demonstrate that ultradense three-dimensional integrated optics is possible in single-mode air-waveguide circuit paths traversing the volume of a 3D optical microchip. Each single-mode waveguide supports an additional "dimension" of wavelength bandwidth of up to 200 nm, centered at a 1.5-μm wavelength, enabling a single circuit to simultaneously process hundreds of wavelength channels of information flow. This "3+1 dimensional" (3+1D) all-optical microchip enables an unprecedented speed and density of information flow and is universally obtainable in almost any 3D PBG material, regardless of architecture.

A functional 3D optical microcircuit is depicted in Fig. 1, consisting of several planar microchip layers[11] linked by vertical waveguides. The 3D microchip enables up to 200-nm single-mode waveguiding in each planar chip layer and 100-nm bandwidth chip-to-chip interconnects in a variety of 3D PBG materials, including woodpiles,[12,13,16] slanted pore architectures,[17,18] and square spiral post arrays.[19,20] We illustrate our 3+1D microcircuit design, with the recently introduced $\mathbf{SP_2}$ slanted pore PBG material.[17,21,22] In Fig. 1, the bottom cladding section consists of four or more unit cells (in depth) of slanted pore 3D PBG material. The $\mathbf{SP_2}$ crystals are defined by a tetragonal lattice with lattice constants c

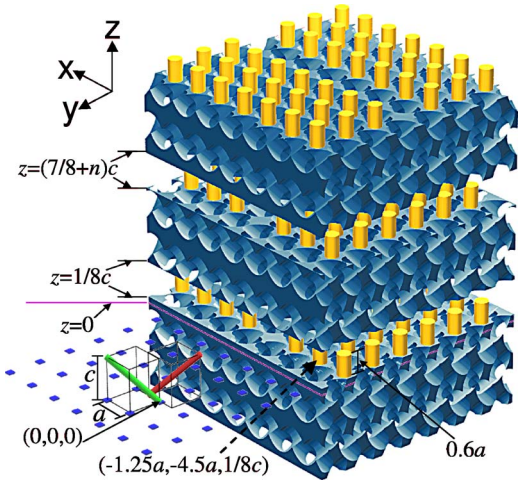

FIG. 1. (Color online) Schematic of a 3+1D optical microchip using the slanted pore 3D PBG material. The bottom, intermediate, and top cladding sections of the microchip (consisting of the slanted pore 3D PBG materials) are separated and intercalated with lattice-matched 2D photonic crystal circuit layers. The first (lowest) planar circuit layer, sitting on the bottom cladding section, is inserted at the plane $z=1/8c$. The planar circuit layer consists of a square lattice of circular rods with a radius of $0.2a$ and a thickness of $0.6a$, with one of the lattice points centered at $(x,y)=(-1.25a,-4.5a)$ for the first layer (dashed arrow). The second planar circuit layer is positioned at the plane $z=(7/8+n)c$, where n is an integer. The plane $z=0$ is marked by magenta (gray) lines. Note that the coordinates z used here refer to positions in the bulk $\mathbf{SP_2}$ material before insertion of 2D photonic crystal circuit layers.

along the z axis and a along the x and y axes. The structure is created by drilling two cylindrical pores of radius, r, along the $(0,0,0)$-(a,a,c) and $(0.5a,0,0)$-$(-0.5a,-a,c)$ directions, displaced from each other in the x direction by $0.5a$, in each unit cell of the square lattice. The $\mathbf{SP_2}$ structure used here has the structural parameters $c=1.2a$, $r=0.28a$, a dielectric volume fraction of 34%, and exhibits a complete PBG of ~17%. We assume the dielectric constant of 11.9, corresponding to that of silicon at 1.5 μm.[23] To place the single-mode waveguide band center at 1.5 μm, the lattice parameters are chosen as $a\sim 540$ nm, $c\sim 650$ nm. The thickness of each 2D photonic crystal layer is $0.6a$. The lowest planar circuit layer is separated from the next planar circuit layer by at least three unit cells (in depth) of the 3D PBG $\mathbf{SP_2}$ structure (only 1.75 unit cells are shown in Fig. 1). The second (middle) planar circuit layer is stacked on top of the 3D PBG separator section and the same process can be repeated to intercalate as many planar microchips as desired. The separator sections and top cladding section are laterally aligned with the bottom cladding sections as follows: If the 2D microchip layers were removed and 3D PBG cladding sections were reconnected by vertical displacement, a bulk $\mathbf{SP_2}$ structure would be reconstituted. The vertical waveguide, connecting microchip layers, has a nearly universal design consisting of the removal of the dielectric, from the regions contained by two rectangular boxes in each unit cell, along a column of such unit cells connecting the adjacent microchip layers [Figs. 2 and 3(a)]. The position of each box is determined by careful examination of the field distribution of photonic modes below the band gap. Each box is, in fact, centered where the field intensity peaks for certain photonic modes below the band gap and extends to where the field intensity is weak. As in the 2D-3D heterostructure design for a single planar microchip,[11,15] the waveguide in the 2D photonic crystal layer is created by removing a row of dielectric rods along the x or y direction of the square lattice. For the current design, the single-mode bandwidth is $(a/\lambda \sim 0.324-0.366)$, 193 nm for the in-plane waveguide and $(a/\lambda\sim 0.335-0.376)$, 175 nm for the vertical interconnect. The overlap bandwidth of $a/\lambda\sim 0.335-0.366$ represents the overall single-mode bandwidth of the 3D circuit path.

We first consider a vertical U-turn circuit path, consisting of forward propagation of light on a 2D microchip waveguide followed by a 90° turn upward along a vertical interconnect and then another 90° turn backward on an adjacent microchip layer (upper part of Fig. 2). The fourfold screw symmetry about the z axis of the $\mathbf{SP_2}$ structure[17] (like the square spiral photonic crystal[19] and the woodpile[16]), requires that the number of unit cells in the separator section is equal to $n+0.75$, where n is an integer. A U-turn in the separator section consists of climbing three out of four segments of the screw within a single unit cell. This imposes a $0.5a$ lateral shift in the upper air waveguide relative to the lower waveguide. Our design rule for the vertical interconnect consists of removing dielectric from the 3D PBG separator section within the boxes shown in red (dark gray) in Fig. 2. To eliminate cross talk between the adjacent 2D microchip layers we use a separator section of thickness 3.75 unit cells. We note that the direction of the magnetic field vector is kept the same for the entire U-turn path (perpendicular to the plane that contains the "U"). In this way, a good connection at the two corners in the U-turn path is ensured by matching of the magnetic field.

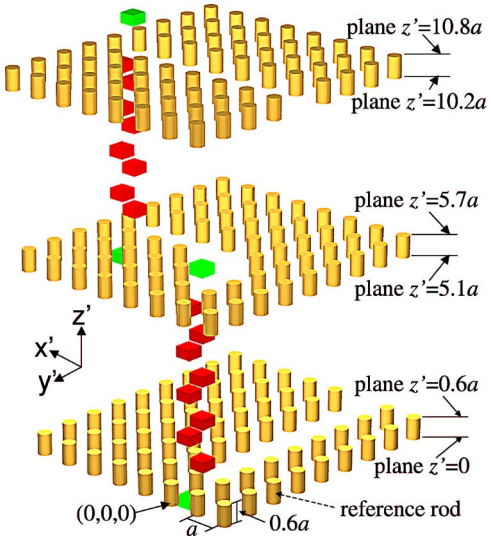

FIG. 2. (Color online) Schematic for the 3+1D optical microchip showing only the 2D photonic crystal microchip layers and the vertical waveguides. In-plane waveguides and bends are patterned in the 2D photonic crystal layers by removing certain dielectric rods. Here, new coordinates (x',y',z') are introduced to describe the 3+1D microchip after insertion of 2D circuit layers, where $x'=x-0.75a$, $y'=y+2.5a$, and the plane $z'=0$ refers to the bottom face of the first 2D layer. Consequently, the origin is shifted to the (bottom face) center of one of the rods as shown by the large black arrow. For reference, the rod marked by the dashed arrow in Fig. 1 is also shown by a dashed arrow here. The first $[z'=0.6a-(0.6a+3.75c)]$ and the second $[z'=(1.2a+3.75c)-(1.2a+7.5c)]$ three-dimensional separator sections correspond to $z=0.125c-3.875c$ and $z=3.875c-7.625c$, respectively. Vertical waveguides (interconnects) are created by removing dielectric from the $\mathbf{SP_2}$ structure within volumes contained by red (dark gray) and green (gray) rectangular boxes. The first (lowest) two red (dark gray) boxes and the lowest green (gray) box are centered at $(0,-1.25a,0.75a)$, $(0.5a,-1.25a,1.35a)$, and $(0.5a,-1.25a,-0.45a)$, respectively.

We use the finite-difference time-domain method (FDTD) with resolution of 10 mesh points per a to calculate the transmission and reflection spectra of the 3D U-turn circuit path. This vertical interconnect acts as a structurally symmetric Fabry-Perot cavity (with three resonant frequencies where the transmission reaches 100% as expected from the mode coupling theory[24]) in the circuit path defined by the U-turn. The off-resonant transmission, however, is determined by the quality (Q) factor of the cavity and is low when the Q factor of the cavity is high. For a high Q factor vertical interconnect, consisting of dielectric removed only from the red (dark gary) boxes shown in Fig. 2, the transmission drops to 25–50 % at the off-resonant frequencies. In order to obtain uniformly high transmission around the U-turn, it is necessary to lower the Q factor of the vertical interconnect.[24] The key step to eliminate backscattering at the vertical wave-

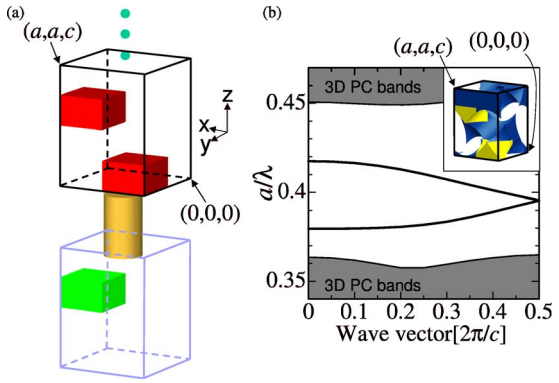

FIG. 3. (Color online) Schematic of the vertical waveguide and its dispersion relation. (a) Within a single unit cell of 3D PBG of size $a\times a\times c$ (black wire box), dielectric material within the two red (dark gray) rectangular boxes is removed. Repeating this process vertically in the $\mathbf{SP_2}$ cladding section, extends the length of vertical waveguide as depicted in Fig. 2. One corner of the bottom face of the unit cell at (0,0,0) corresponds to $(x',y',z')=(-0.25a, -2a, 0.6a)$ in Fig. 2. The size of the red (dark gray) and green (gray) boxes is $0.5a\times 0.5a\times 0.25c$ in the x, y, and z directions, respectively. The two red (dark gray) boxes are centered at $(0.25a, 0.75a, 0.15a)$ and $(0.75a, 0.75a, 0.75a)$, respectively. Below the first and above the second 2D microchip layers, dielectric material within the green (gray) boxes is also removed. The green (gray) box below the first 2D layer is centered at $(0.75a, 0.75a, -1.05a)$. (b) The dispersion relation for the vertical waveguide in the bulk $\mathbf{SP_2}$ material created by periodically repeating the unit cell (black wire box) shown in (a). The single mode waveguide dispersion relation that spans the frequency range of $a/\lambda\sim 0.335-0.376$ is plotted as a solid black curve. This corresponds to a vertical waveguiding bandwidth of $\sim$175 nm near the wavelength of 1.5 μm. The inset shows the actual dielectric structure of the vertical waveguides. The blue (dark gray) parts correspond to dielectric material of the $\mathbf{SP_2}$ structure. The yellow color (gray) indicates dielectric material removed to create a vertical waveguide, which correspond to the volumes inside the red (dark gray) boxes shown in (a).

guide bend is the removal of additional dielectric from the top and bottom $\mathbf{SP_2}$ cladding sections throughout the green (gray) boxes depicted in Fig. 2. This extension of the vertical waveguide above and below the 2D microchip layers is a universal mechanism for achieving large bandwidth chip-to-chip interconnection in PBG materials. The final structure exhibits a uniformly high transmission (>94%) for the U-turn over the frequency range $a/\lambda\sim 0.335-0.357$ as shown by red (solid) lines in the inset of Fig. 4 (bandwidth of $\sim$100 nm near 1.5 μm). For a thicker 3D PBG separator section of thickness 7.75 unit cells, the transmission [shown by blue (broken) lines in the inset of Fig. 4] exhibits more peaks as would be expected in a Fabry-Perot resonator with a long cavity length. Likewise, the Q factors increase with thicker separator section, as commonly found in Fabry-Perot resonators. Nevertheless, high transmission of >90% is maintained throughout the single-mode waveguiding overlap bandwidth. It is likely that further refinement[25] of the vertical elbow design would improve the transmission characteristics even further.

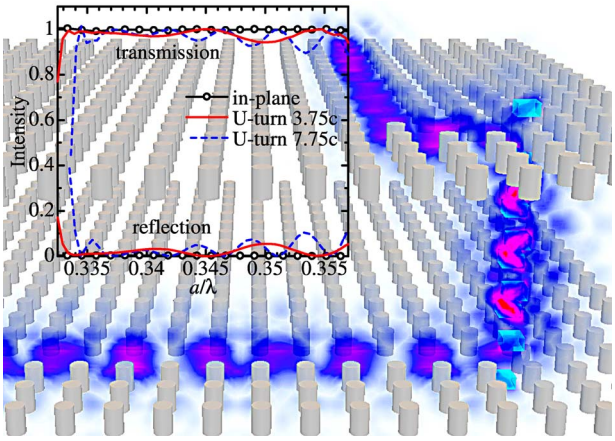

FIG. 4. (Color online) Poynting vector intensity of light (frequency $a/\lambda=0.345$) propagating along the combined vertical bend (U-turn) and in-plane 90° bend, for the $\mathbf{SP_2}$-based 3D microchip, obtained by FDTD simulation. The blue (black) and magenta (gray) shading corresponds to small and large magnitudes of the Poynting vectors at a particular instant, respectively. Only the structure of the two 2D photonic crystal layers (gray cylinders) and the vertical waveguides (bright rectagular boxes of removed dielectric) are shown. The inset shows transmission and reflection spectra of two vertical U-turn bends, the first with a vertical interconnect of length $3.75c$ [red (solid)] and the second with length $7.75c$ [blue (broken)]. The corresponding spectra for a simple 90° in-plane bend are superimposed (black lines with circles). There is minimal reflection around the U-turn, throughout the entire single-mode bandwidth (of $\sim$100 nm) of the circuit.

More complex circuit paths are easily obtained by combining the vertical U-turn interconnect with other in-plane waveguide apertures. A simple nonplanar circuit path (depicted in Fig. 4) is obtained by combining the vertical U-turn with an in-plane 90° bend. Our FDTD calculations reveal that the transmission spectrum of the 3D circuit path is comparable to that of the vertical U-turn interconnect alone. The top right inset of Fig. 4 shows the transmission and reflection spectra (white lines with circles) for a 90° bend within the 2D photonic crystal layer, where almost 100% transmission is obtained over the same range of frequency.[11,15] Clearly, our 3D chip architecture allows the embedding of a variety of previously established[26] 2D circuitry within each planar microchip layer with equal and sometimes improved functionality. We have verified numerically that essentially the same design rules can be applied to other 3D PBG materials such as the woodpile and the square spiral, yielding similar 3D circuit characteristics.

Three-plus-one-dimensional circuit architectures can be implemented with technologies currently used to fabricate 3D PBG materials. Micromachining technologies[27,28] may be used to fabricate the woodpile-based 3+1D circuit. The $\mathbf{SP_2}$ or square spiral-based circuits may be realized in template form by the direct laser writing[22,29] in polymer photoresists. The templates can then be replicated with high-index semiconductors, such as silicon, using a double inversion process consisting of (i) room temperature chemical vapor deposition (CVD) of SiO_2, (ii) selective removal of the photoresist,

(iii) CVD of silicon, and (iv) selective removal of the SiO_2 daughter template. High-bandwidth optical circuitry written into a 3D PBG microchip combined with active devices on chip[30] may provide unprecedented compactness, information density, and processing speed for future optical communications and computing.

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