ANALOG DEVICES

DDS DAC Output Evaluation Board
AD9858PCB

INTRODUCTION

The AD9858 is a 1 GHz direct digital synthesizer (DDS) featuring a 10-bit DAC, an RF mixer, and on-chip PLL synthesis blocks. Used in conjunction, the various components of the AD9858 allow the user to construct translation loops (also known as offset loops), fractional divider loops, traditional integer-N PLL loops, as well as frequency synthesis directly from the DDS. Because different systems require different connections and different external components, each evaluation board was designed with a specific application in mind. This document addresses the evaluation board that allows each of the frequency synthesis blocks to be used or left unused at the discretion of the user. Included within is information on system requirements, installing the evaluation software, menus and buttons, and window environments. Documentation for the other boards (fractional-divide loop and translation loop) is also accessible from the Design Tools section of the Analog Devices DDS homepage: www.analog.com/dds.
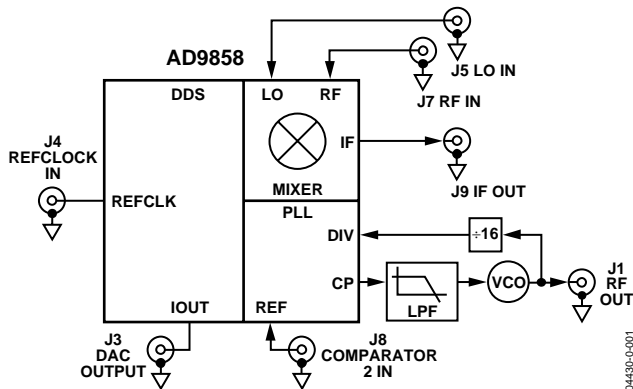

Figure 1. AD9858 DAC Output Evaluation Board

CIRCUIT OVERVIEW

The DAC-output evaluation board was designed to allow the user full control over some or all of the functional blocks of the AD9858. Each of the functional blocks has its inputs and outputs brought on and off board separately. Users can configure and connect the DDS block, the PLL block, and the mixer block in whatever fashion they wish, bounded by the parametric limitations of the device. For example, if a user wished to only evaluate the RF mixer, the external reference (REFCLK) to the DDS core and the PLL inputs could be left unconnected. This allows the user to evaluate the performance of the mixer as an individual component.

The DAC output board allows for external REFCLK signals up to 2 GHz. For REFCLK signals between 1 GHz and 2 GHz, the on-chip clock divider (divide-by-2) must be used. The user has control over the output frequency by adjusting the tuning word of the DDS. The frequency tuning word and reference clock determine the output frequency of the DDS according to the following equation:

$$F_o = \frac{FTW \times REFCLK}{2 \times 2^N}$$

given that $0 \leq FTW \leq 2^{31}$ and N is the number of bits in the turning word. For the AD9858, N = 32.

This equation is for the DDS operating with the divide-by-2 function enabled on the REFCLK path (which is the default setting). When the divide-by-2 function is not enabled, the divisor is simply 2^N. The unfiltered output of the DDS is supplied to the user via an SMA connection.

To evaluate the phase detector/charge pump block, the reference input of the phase detector (labeled 'comparator 2 in' on the evaluation board schematic) can be accessed. The output of the PLL block, the charge pump output signal, is fed to the loop filter included on the evaluation board. The filtered charge pump output signal drives the included VCO. The output frequency of the VCO varies between 1530 MHz and 1630 MHz and is available via the RF Out connector. The RF Out signal is divided by 16 and fed back to the other phase detector input.

To evaluate the on-chip RF mixer, users can access the inputs (RF_{in}, LO_{in}) and the output (IF_{Out}). To build different applications, the DDS, the PLL block, and the RF mixer block can be interconnected with SMA cables. Thus, the output of the PLL block, RF Out, could be used as the REFCLK for the DDS (if the divide-REFCLK-by-2 function of the DDS is enabled).

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REVISION HISTORY

Revision 0: Initial Version

EQUIPMENT

In order to install and use this software and evaluation board, the user needs the following:

2   Power supplies

1   PC (Windows® 95 or higher), with one free parallel printer port

1   Precision signal generator (to act as a stable clock source)

1   Spectrum analyzer for viewing the output waveform

Miscellaneous cables

INSTALLING FROM THE CD

1. Insert the CD-ROM into the CD drive.

2. On your desktop, open Windows Explorer.

3. Locate the setup.exe file.

4. Double-click the file and follow the instructions.

INSTALLING FROM THE WEB

1. From your browser, go to www.analog.com/dds.

2. Click the product selection guide link.

3. Click the AD9858 link, then click the design tools link.

4. Click the install evaluation software link and follow the instructions that appear.

After starting the AD9858 evaluation software, the main program window appears. At the top of the screen are the File, PC I/O, View, and Help menus and the Load Setup, Save Setup, Reset, I/O Config, and FUD buttons.
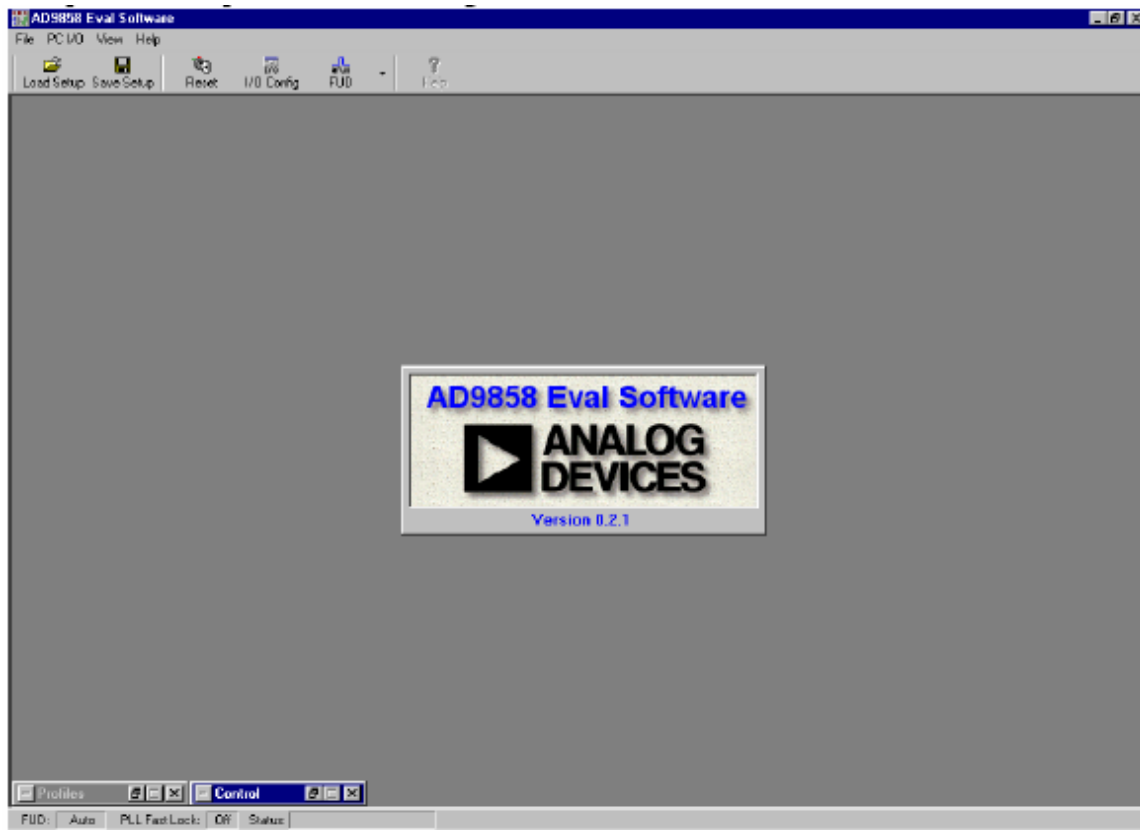
MAIN PROGRAM WINDOW

Figure 2. Main Program Window

BUTTONS

The main program window has these buttons:

- The Load Setup and Save Setup buttons load a setup file and save the current setup to a setup file.

- The Reset button issues a master reset to the device (all registers are cleared and return to default values).

- The I/O Config button displays the I/O Config Interface where the user can specify whether to communicate with the device in parallel or serial mode. (The PC always communicates with the evaluation board in parallel mode).

- The FUD (Frequency Update) button issues a frequency update signal to the device. This updates the digital data being used by the DDS core to the current values stored in memory. Note that a submenu appears when the FUD button is clicked, allowing the user to specify whether the program should automatically issue FUDs or wait for the user to click the button.

MENUS

The AD9858 evaluation software is a menu-driven interface. This section describes the menus and associated commands.

File

Figure 3. File Menu

From the File menu, the user may load an existing setup, save the current setup, or exit the software.
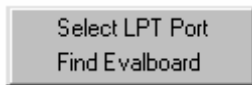
PC I/O

Figure 4. PC I/O

From this menu the user may

- Specify which port to use to communicate with the evaluation board, if there is more than one parallel port.

- Find the evaluation board that tells the computer to run a handshaking routine, confirming the presence of a functioning evaluation board.
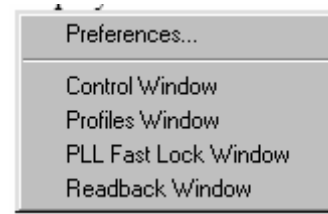
View

Figure 5. View Menu

This menu allows the user to display various interface windows. Brief descriptions are given below for each of these windows, with detailed sections following.

- In the Preferences window, users can change the display color.
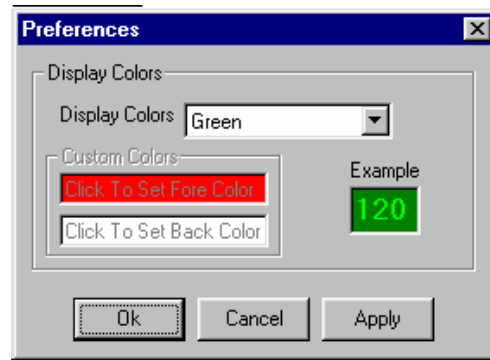

Figure 6. Preferences

- In the Control window, the user programs information about the clock, the power-down features, and the output options. The user can also set miscellaneous control register flags here.

- The Profiles window shows the current values for each of the user-defined profiles, allows the user to click a name to select a profile, and enables the user to set the parameters for frequency sweeping.

- The PLL Fast Lock window can be used to specify whether the device should use the PLL Fast Lock algorithm, and if so, what parameters it should incorporate into that algorithm.

- The Readback window displays all data currently programmed into the AD9858-memory registers.

Help

Figure 7. Help Menu

An online help feature will be added in the future.

CONTROL WINDOW

The control window allows the user to set many of the operating parameters of the device. In the Clock pane, the user can specify the current clock frequency supplied to the device. If the user desires, the clock divide-by-2 feature may be enabled. After selecting this option, the user must click the LOAD button. Until the LOAD button is clicked, it flashes green indicating that a data change has been made but not loaded yet. The clock divide-by-2 must be enabled for any clock frequency exceeding 1 GHz.

To conserve power, the user may power down different subsystems on the device, or perform a full power-down.

Under the Output Options pane, users may specify whether they want a sine or cosine output. This is also where the user enables frequency-sweeping mode, although the parameters for the frequency sweep are edited in the profiles screen.

To the right are check boxes that control different bits to be set or cleared in the control register. The auto clear frequency accumulator and auto clear phase accumulator bits work as follows. When set, upon receiving a FUD, the frequency and

phase accumulators are cleared. Then, the frequency and phase accumulators begin accumulating at whatever rate is stored in the delta frequency tuning word (frequency accumulator) and the frequency tuning word (phase accumulator). When this bit is not set, changes to the frequency and phase accumulators are made in association with the values already stored there. The load delta freq. timer specifies whether the device should wait for a FUD signal before internally updating the value stored for the delta frequency ramp rate word (box checked) or whether it should automatically load new delta frequency ramp rate words (box cleared). The clear frequency accumulator bit resets the frequency accumulator and holds the value at zero until this bit is cleared. The clear phase accumulator resets the phase accumulator and holds the value at zero until the bit is cleared. The SYNC clock Out disable pin causes the SYNC clock output stage to be disabled and the pin to become high impedance. The SYNC clock circuitry is still functioning internally, and the SYNC clock signal can be re-enabled when this bit is cleared.

At the bottom of the screen are buttons that open the I/O Interface window and the PLL Fast Lock window.
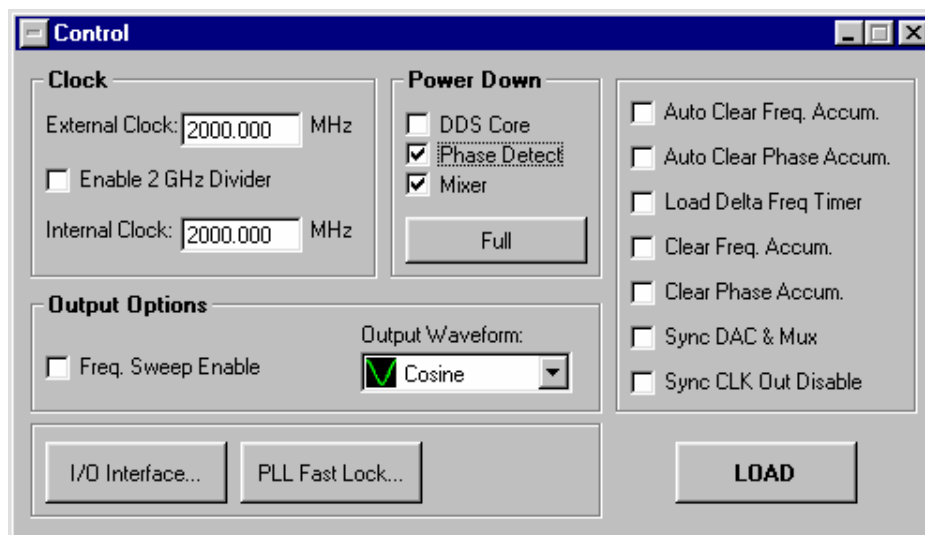

Figure 8. Control Window

I/O INTERFACE

This window is where the user specifies whether the evaluation board is to communicate with the AD9858 device in parallel or serial mode. In serial mode, the user can also specify LSB first or last as well as whether the board should use 2-wire or 3-wire serial communication. During serial communications, it is possible that a communication error can cause a lack of synchronization between the source and the receiver. The I/O reset button can be used to reset the serial port and then reinitiate a communication sequence.
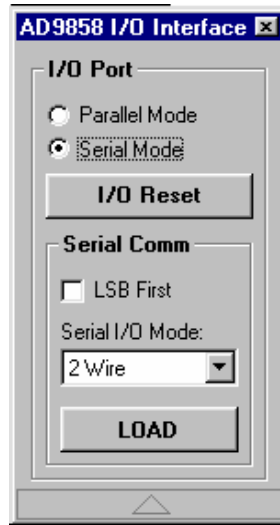
Figure 9. I/O Interface

PLL FAST LOCK

This window is accessible from the Control window or from the View menu. The PLL Fast Lock window allows the user to enable and disable the PLL Fast Lock algorithm. When engaged, the charge pump operates in three modes: a frequency detect mode, a wide closed-loop mode, and a final closed-loop mode. The user programs the charge pump reference current with an external resistor from CP_Iset to ground. Here, the user tells the program what value is used (2400 Ω is the default value on the evaluation board) and then programs the scaling factors the device should use for the different modes. The user can also set the Phase Detector divider ratio. This divisor scales the divider input in time.

Figure 10. PLL Fast Lock Window

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PROFILES WINDOW

The AD9858 has four user-defined profiles (segments of memory). Each profile can be programmed with a different frequency tuning word and phase adjustment word. As shown in Figure 12, users can click the Edit button next to any value for a dialog window in which frequency and phase information may be entered.

While the value is displayed on the screen, it is not yet loaded to the device. To load the information, the user must click the Load button. This button flashes after one or both of the variables in a profile is changed, and continues to flash until the data is loaded. Entering and loading data does not automatically cause the DDS to change to the most recently addressed profile. In order to change profiles, the user must click the profile name, which turns from a dark green to a bright green to indicate that it has been selected as the current profile.

Figure 11. Profiles Window

FREQUENCY SWEEP SETUP DIALOG BOXES

At the bottom of the Profiles window is the display for the frequency sweeping mode variables—Delta Frequency Tuning Word and Ramp Rate. Clicking the Edit button opens a dialog window that assists the user in entering the information. This data is not loaded until the LOAD button is clicked. When unloaded changes have been made, the LOAD button flashes green until the data is loaded.
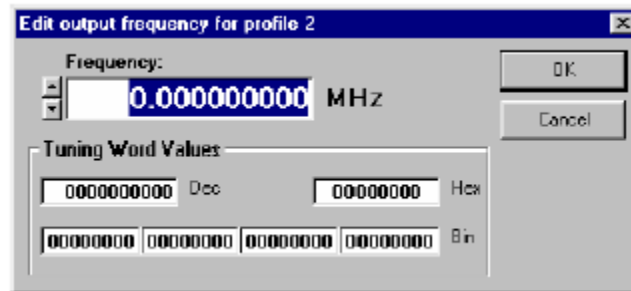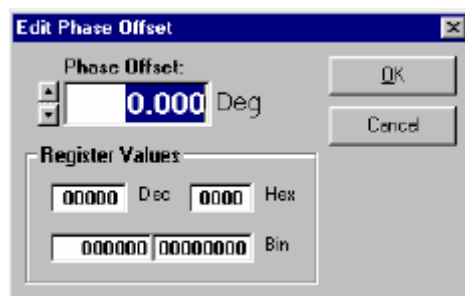

Figure 12. Edit Output Frequency Dialog Box

Figure 12. Edit Phase Offset Dialog Box

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READBACK WINDOW

When the READBACK button is clicked, the evaluation software polls and displays the current contents of all internal memory registers. When the CLEAR button is clicked, a master reset is issued and all internal memory registers are cleared.

Figure 13. Readback Window

USING EVALUATION SOFTWARE WITH THE DAC OUTPUT BOARD

As mentioned in the Circuit Overview section, the AD9858 cannot operate at speeds greater than 1 GHz. It can accept clocks from 1 GHz to 2 GHz, but to do so the divide-clock-by-2 function must be enabled (it is toggled on by default at power-up and after a reset). The clock frequency must be set to the value the user supplies as the external reference; if the value is greater than 1 GHz and less than 2 GHz, leave the divide-by-2 box checked. To bypass the divider, clear the box and load the information. Once the divide-by-2 function is enabled or disabled, the user must program the Icpo currents supplied by the charge pump. (For more information on the different output currents supplied by the charge pump, please see the AD9858 data sheet on the DDS website www.analog.com/dds. The next step in programming the device is to set the frequency of the DDS. Any or all of the four profiles can be used. Load the frequency value into the frequency tuning word for the desired profile, click LOAD, and then click UPDATE.

ELECTRICAL CONNECTIONS

Power Plug Connections

- AVDD = CMOS power (3.3 V)

- DVDD = CMOS power (3.3 V)

- VCC= Bipolar power (3.3 V)

- 5 V = Charge Pump Power (5 V)

- GND

SMB for VCO: SMB to separate 5 V.

Other Connections

- External Reference (SMB from Reference Source)

- RF Out(SMB to Spectrum Analyzer)

- Sync Clock (if desired, SMB to external hardware)

- Data port (parallel printer cable to PC's parallel port)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

AD9858PCB

ORDERING GUIDE

Model	Package Description
AD9858/PCB	Frequency Synthesizer Board

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www.analog.com