White Wires:
1) Cut PC4 trace and jumper to PC5 (PC4 defaults to all out 0 as TXB).
Notes:
1) FPGA configuration is Active Serial with ISP, JTAG and Standard PDK.
2) Layout is for EP3C25T144 but can fall back to smaller versions if unused I/Os are tristated.
3) Configure display for RS232 by removing jumpers R1 and R2 on display.
4) TTL input 70 Ohm termination is intentional to match newer A00s.