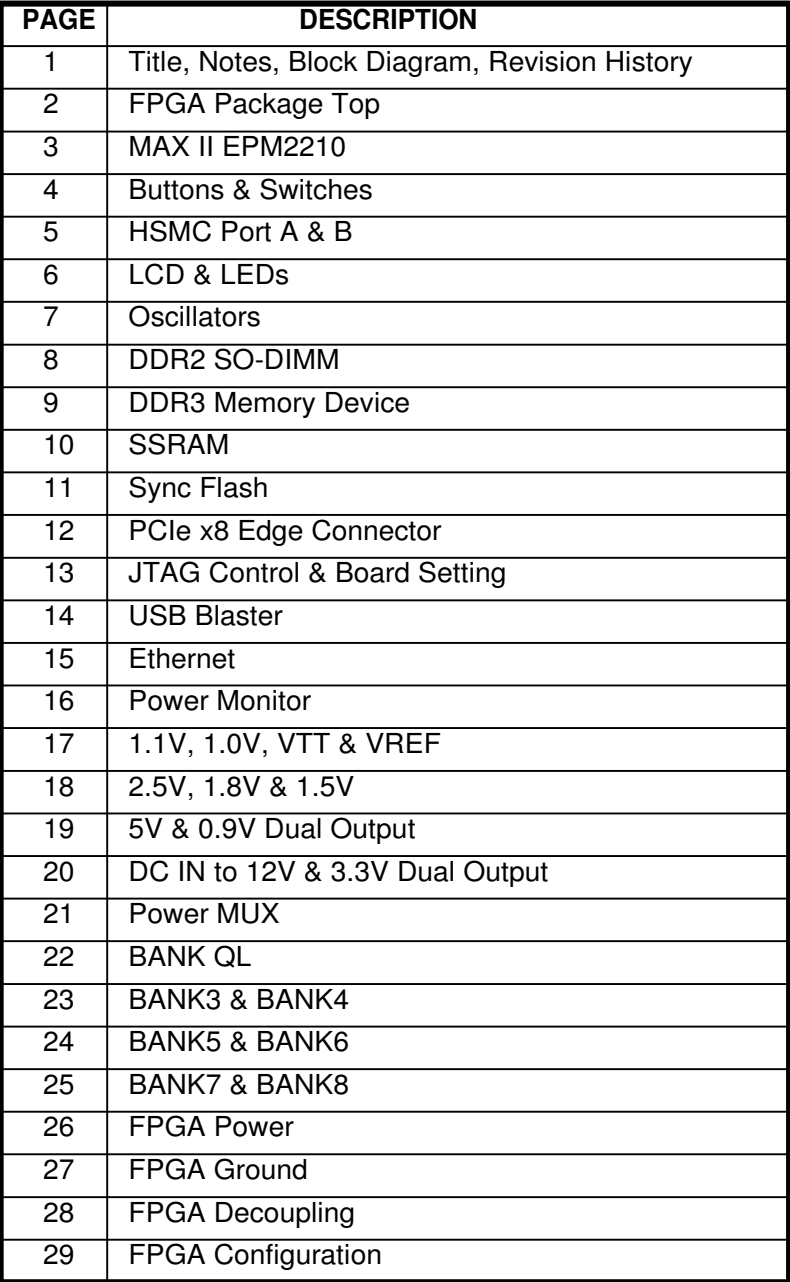


1. Project Drawing Numbers:	
Raw PCB	100-0320801-C1
Gerber Files	110-0320801-C1
PCB Design Files	120-0320801-C1
Assembly Drawing	130-0320801-C1
Fab Drawing	140-0320801-C1
Schematic Drawing	150-0320801-C1
PCB Film	160-0320801-C1
Bill of Materials	170-0320801-C1
Schematic Design Files	180-0320801-C1
Functional Specification	210-0320801-C1
PCB Layout Guidelines	220-0320801-C1
Assembly Rework	320-0320801-C1

Arria II GX FPGA Development Kit Board



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FPGA Package Top View

BANK 7A

VCCIO = 1.5V

DDR3 Device (128MB)

BANK 7B, 8A

VCCIO = 2.5V

ENET, FSM Bus, SSRAM

BANK 6B

(EP2AGX260 only)

VCCIO = 2.5V

HSMC Port B

BANK 6A

VCCIO = 2.5V

HSMC Port A,
Flash Control, FSM Address,
LCD, DIP Switch, LEDs,
PCIe Control

BANK 5A

VCCIO = 2.5V

HSMC Port A

BANK 5B

(EP2AGX260 only)

VCCIO = 2.5V

HSMC Port B

BANK 4B

VCCIO = 1.8V

DDR2 SODIMM x64
Push-buttons

BANK 4A & 3A

VCCIO = 1.8V

DDR2 SODIMM x64

BANK 3B

(EP2AGX260 only)

VCCIO = 2.5V

HSMC Port B

Notes:

- FPGA Schematic Symbol Breakdown:
 - (A) Banks 3A
 - (B) Banks 3B (EP2AGX260)
 - (C) Banks 4A,4B
 - (D) Banks 5A
 - (E) Banks 5B (EP2AGX260)
 - (F) Banks 6A
 - (G) Banks 6B (EP2AGX260)
 - (H) Banks 7A,7B
 - (I) Bank 8A
 - (J) Clocks
 - (K) Configuration
 - (L) Power
 - (M) IO Power
 - (N) GND1
 - (O) Transceivers
 - (P) Transceiver Power
- Board can support the EP2AGX125EF35 and EP2AGX260EF35 devices.

XCVR BANK QR3 (EP2AGX260 only)

HSMC Port B x4

XCVR BANK QR2

HSMC Port A x4

XCVR BANKS QL0, QL1

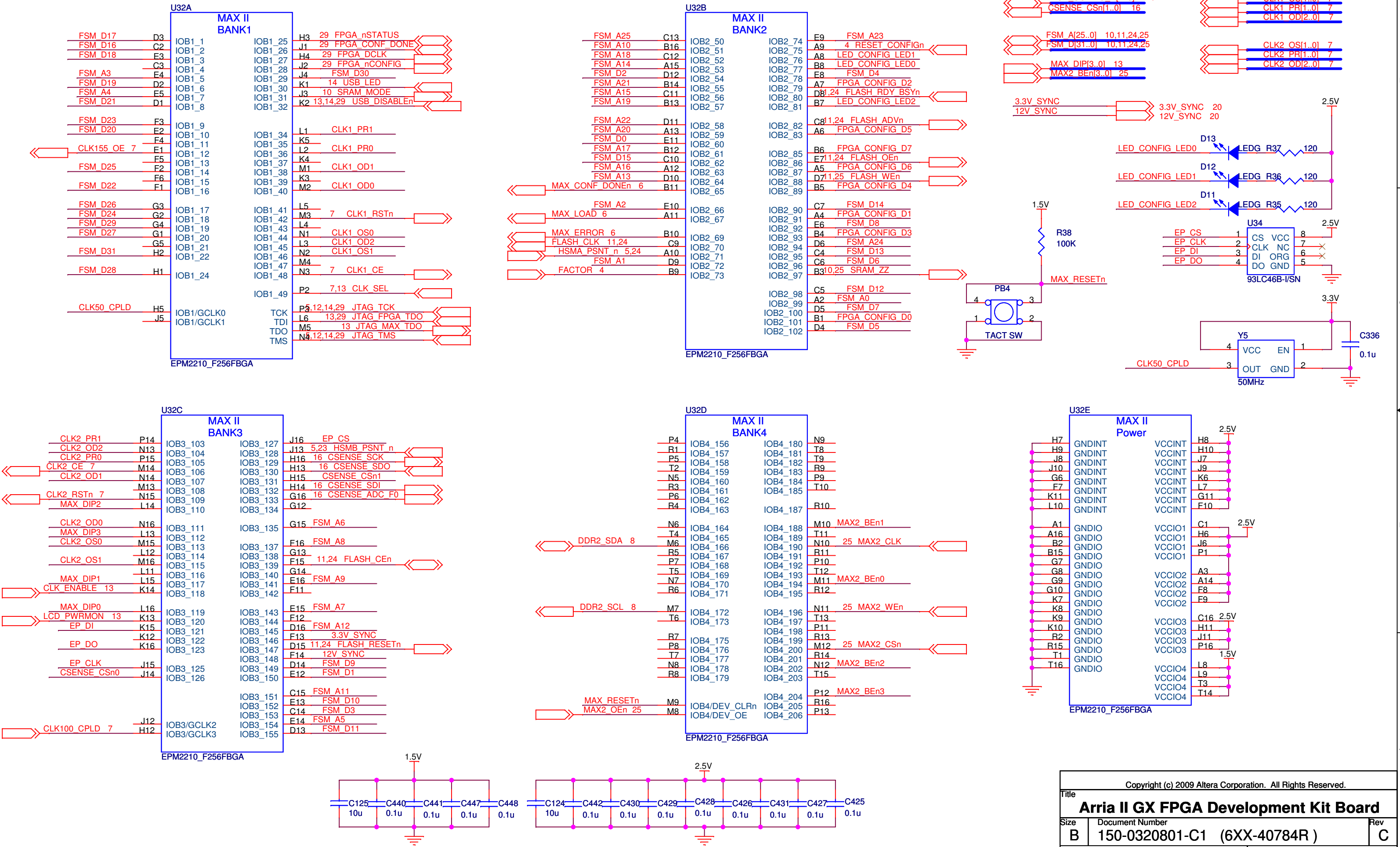
PCI Express x8

PCIe REFCLK

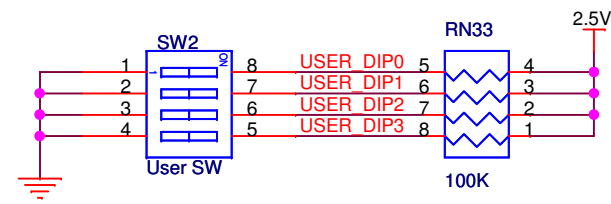
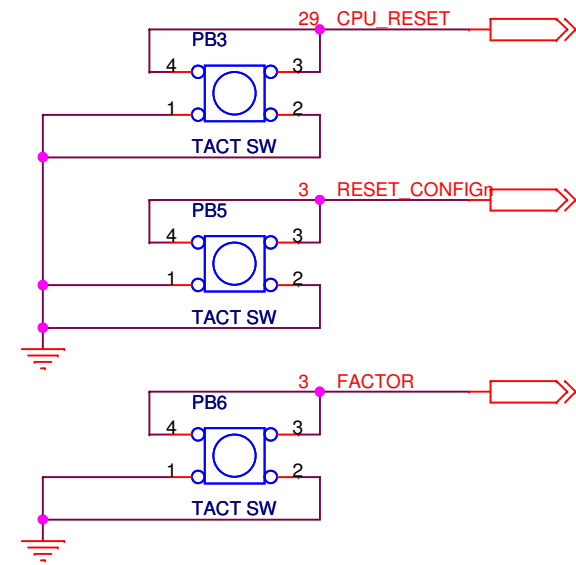
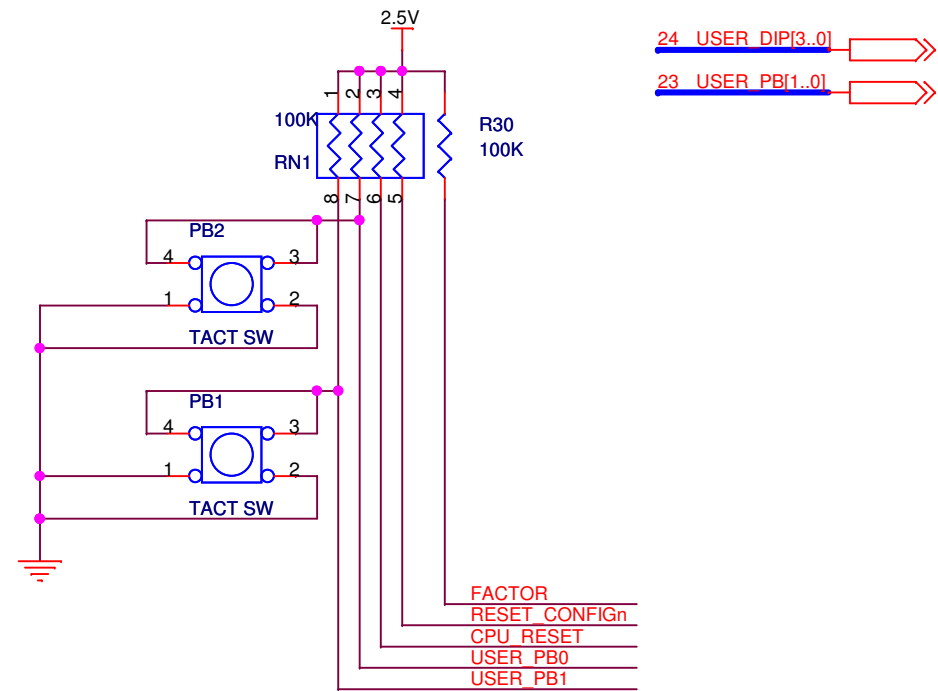


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Title Arria II GX FPGA Development Kit Board		
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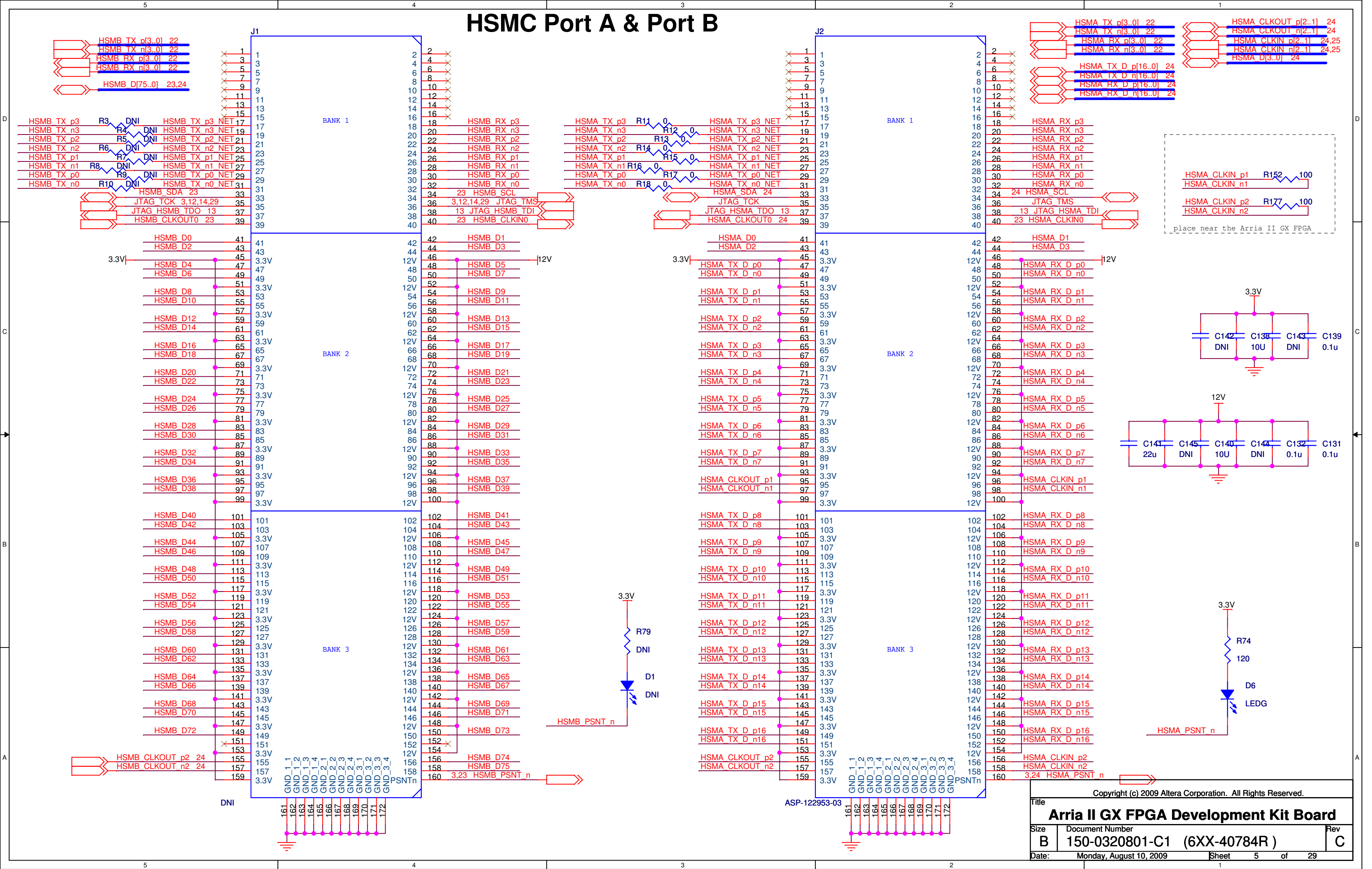
MAX II EPM2210



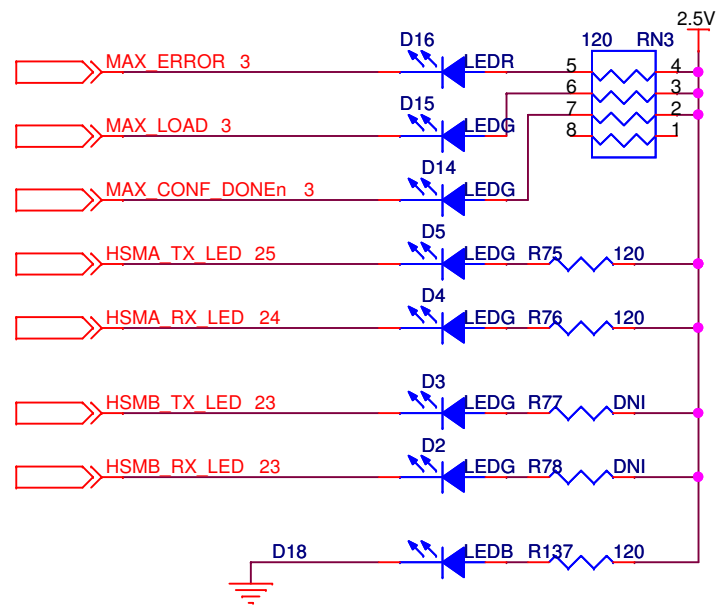
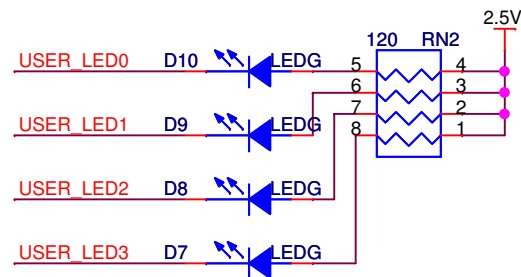
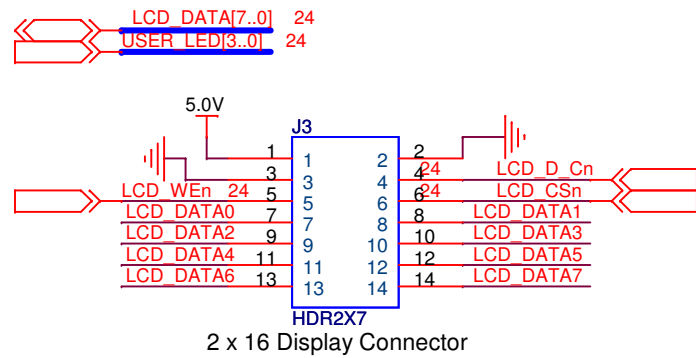
Buttons & Switches



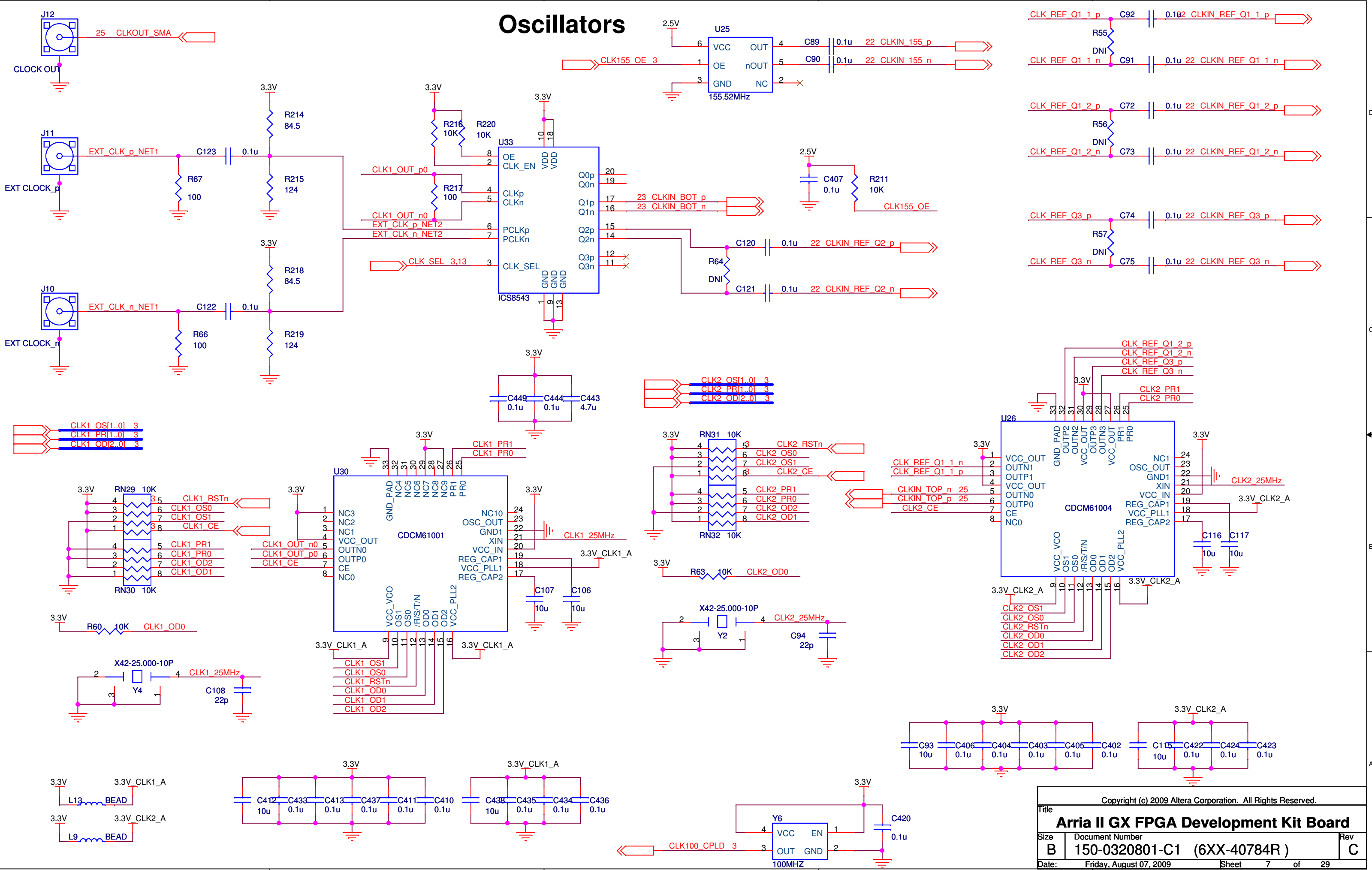
HSMC Port A & Port B



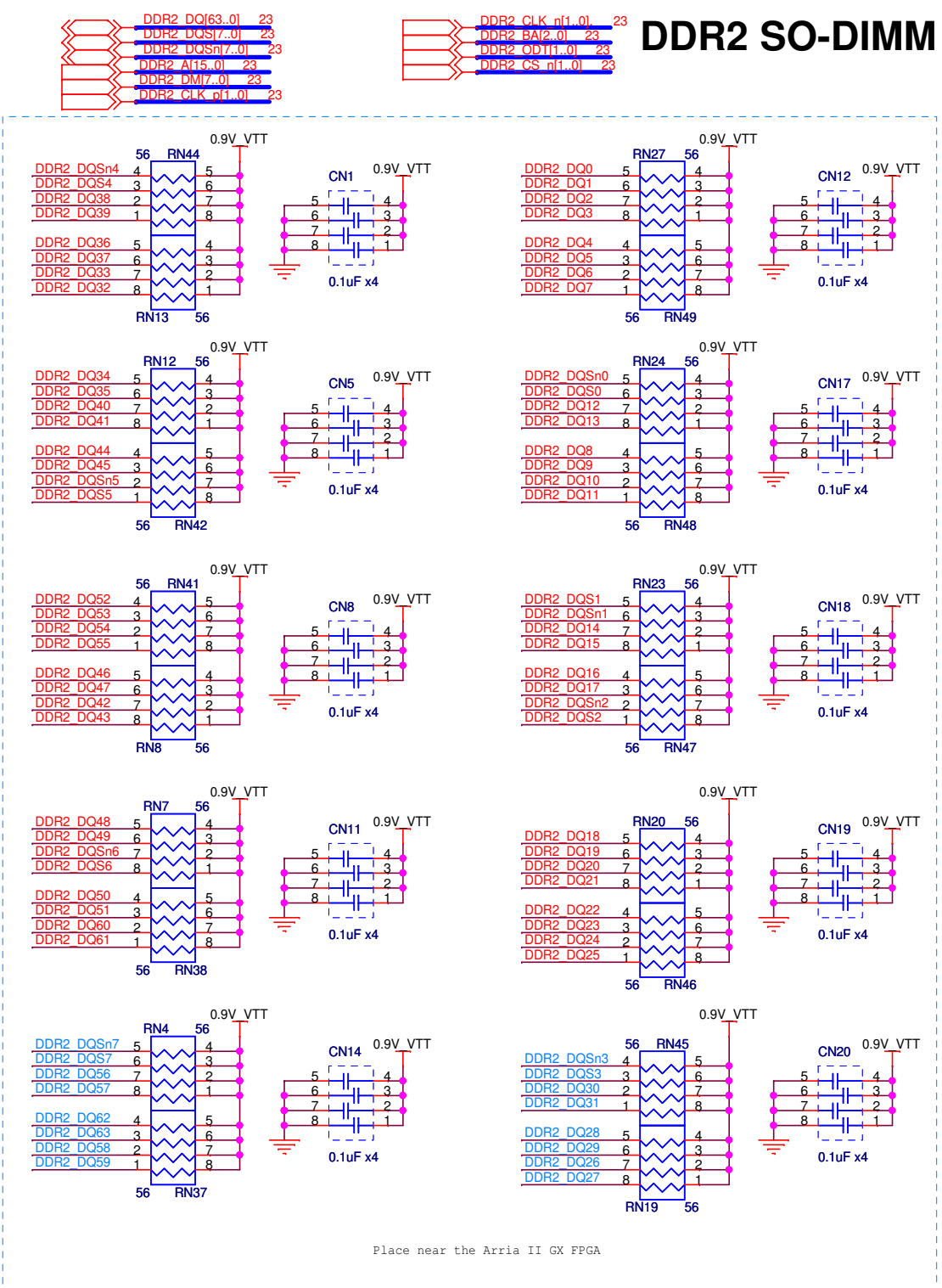
LCD & LEDs



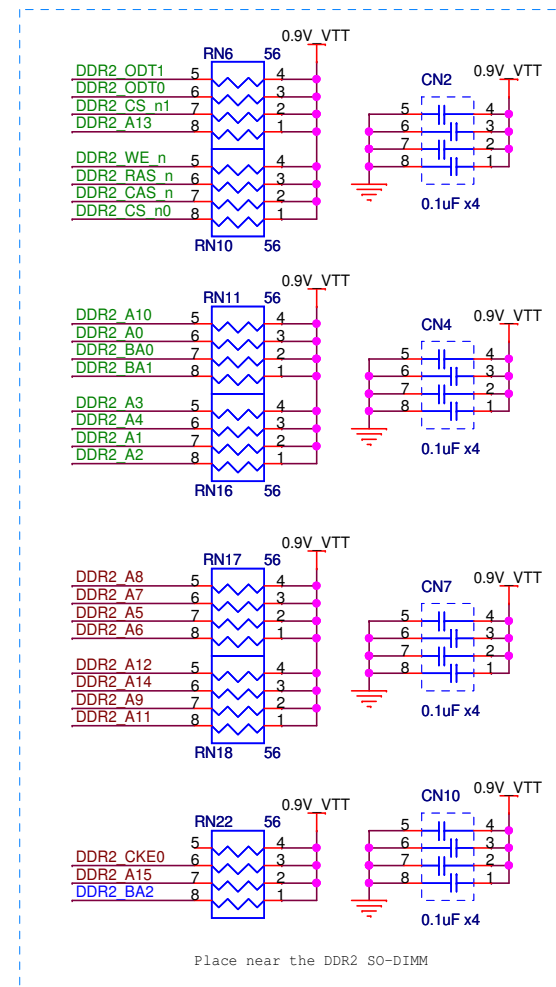
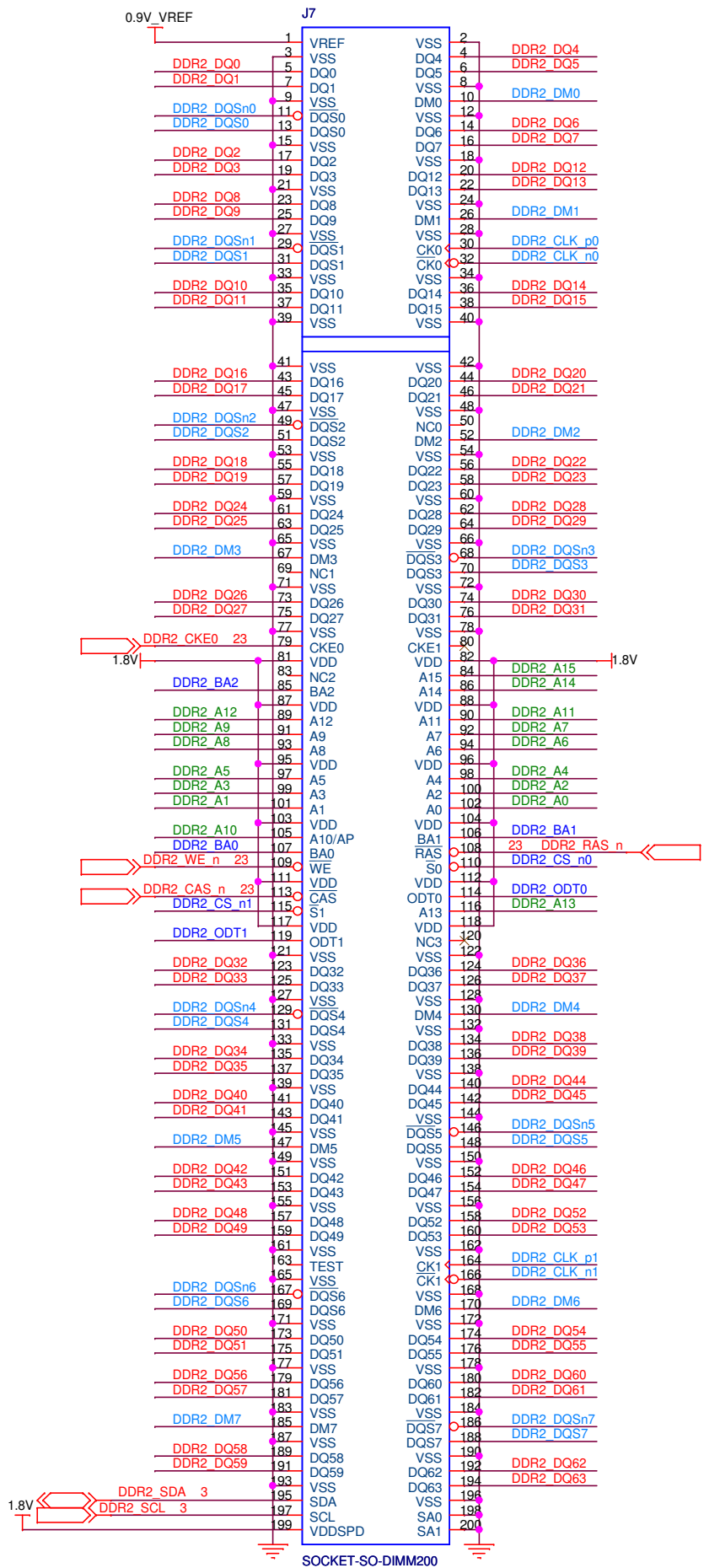
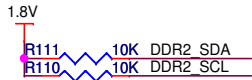
Oscillators



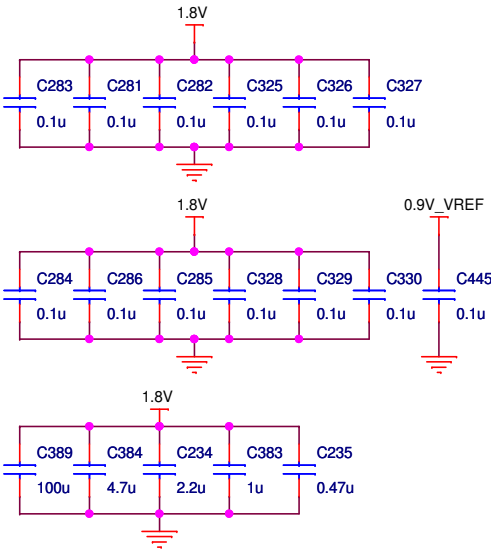
DDR2 SO-DIMM



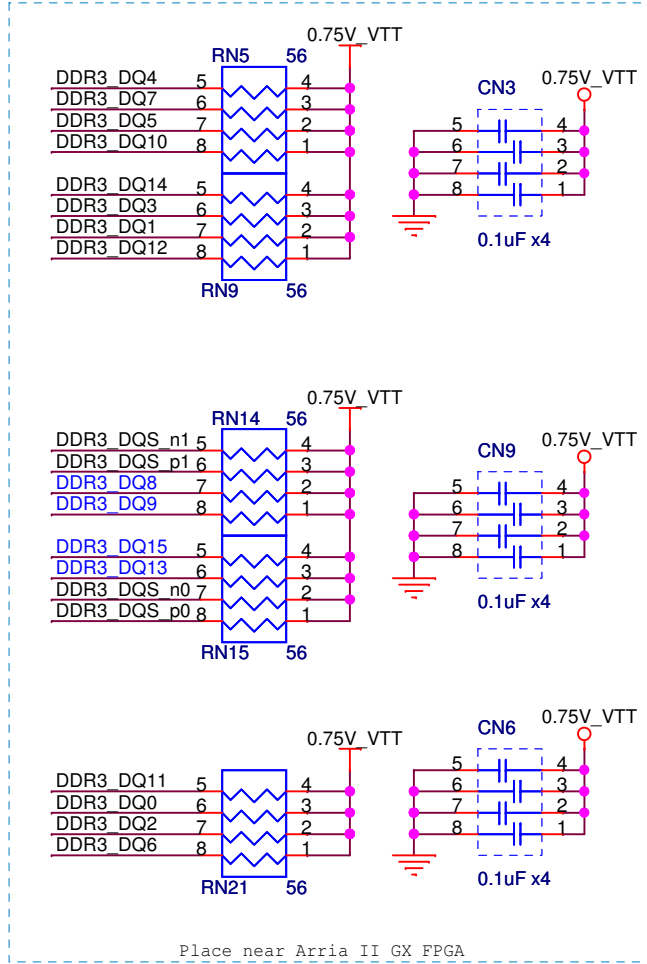
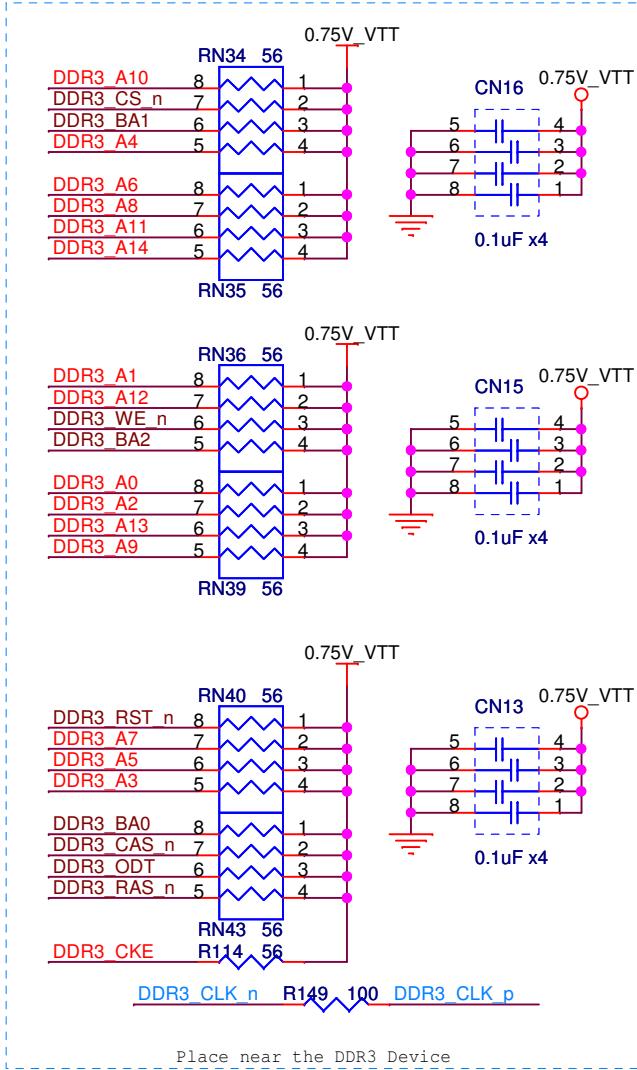
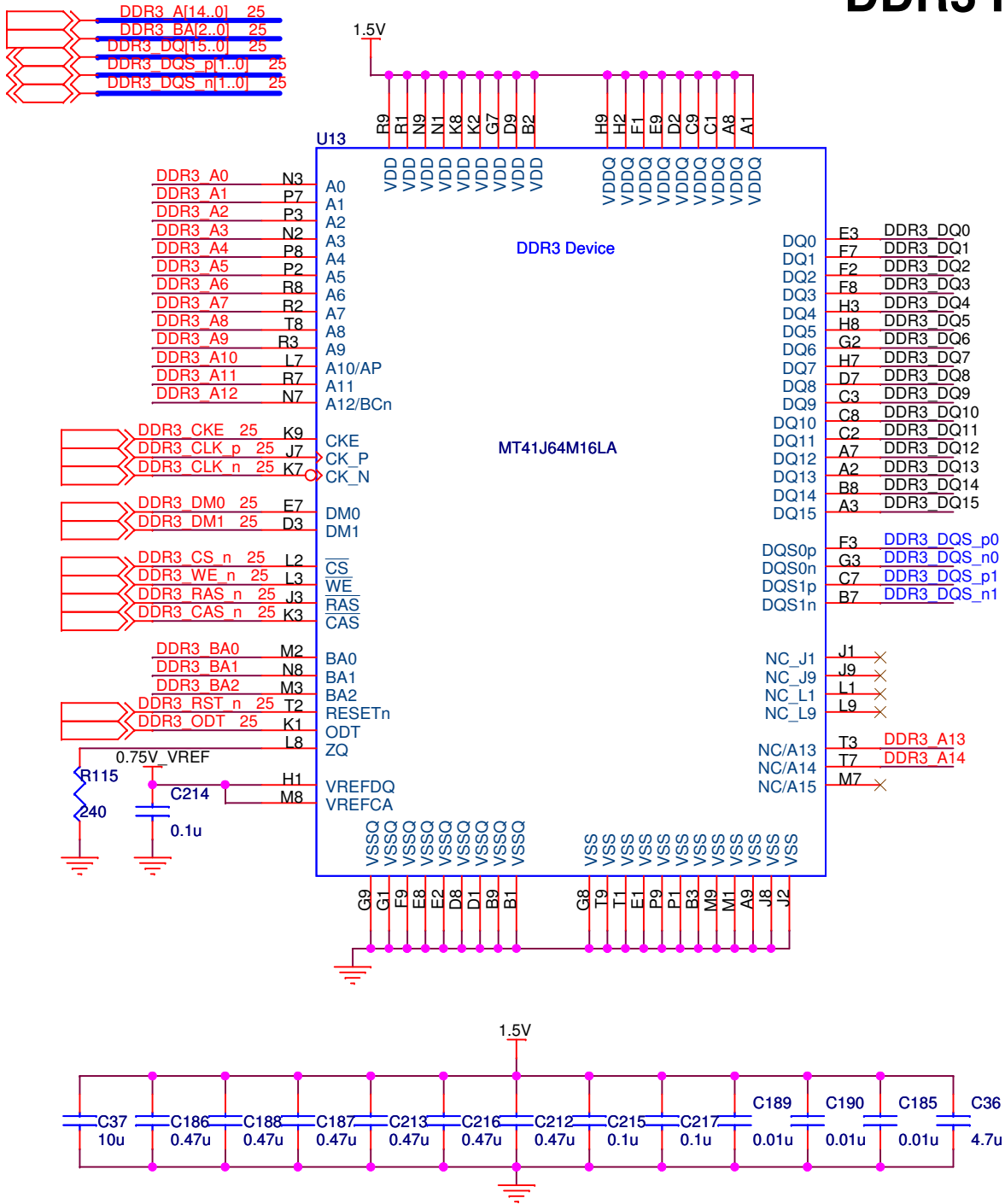
Place near the Arria II GX FPGA



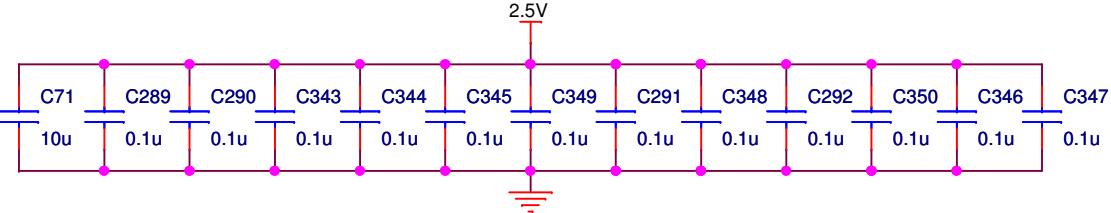
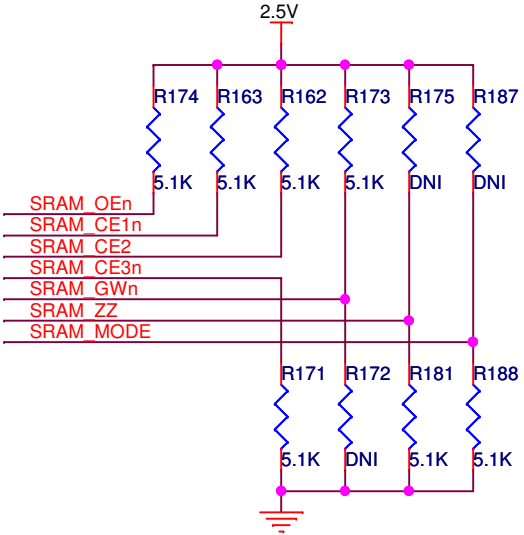
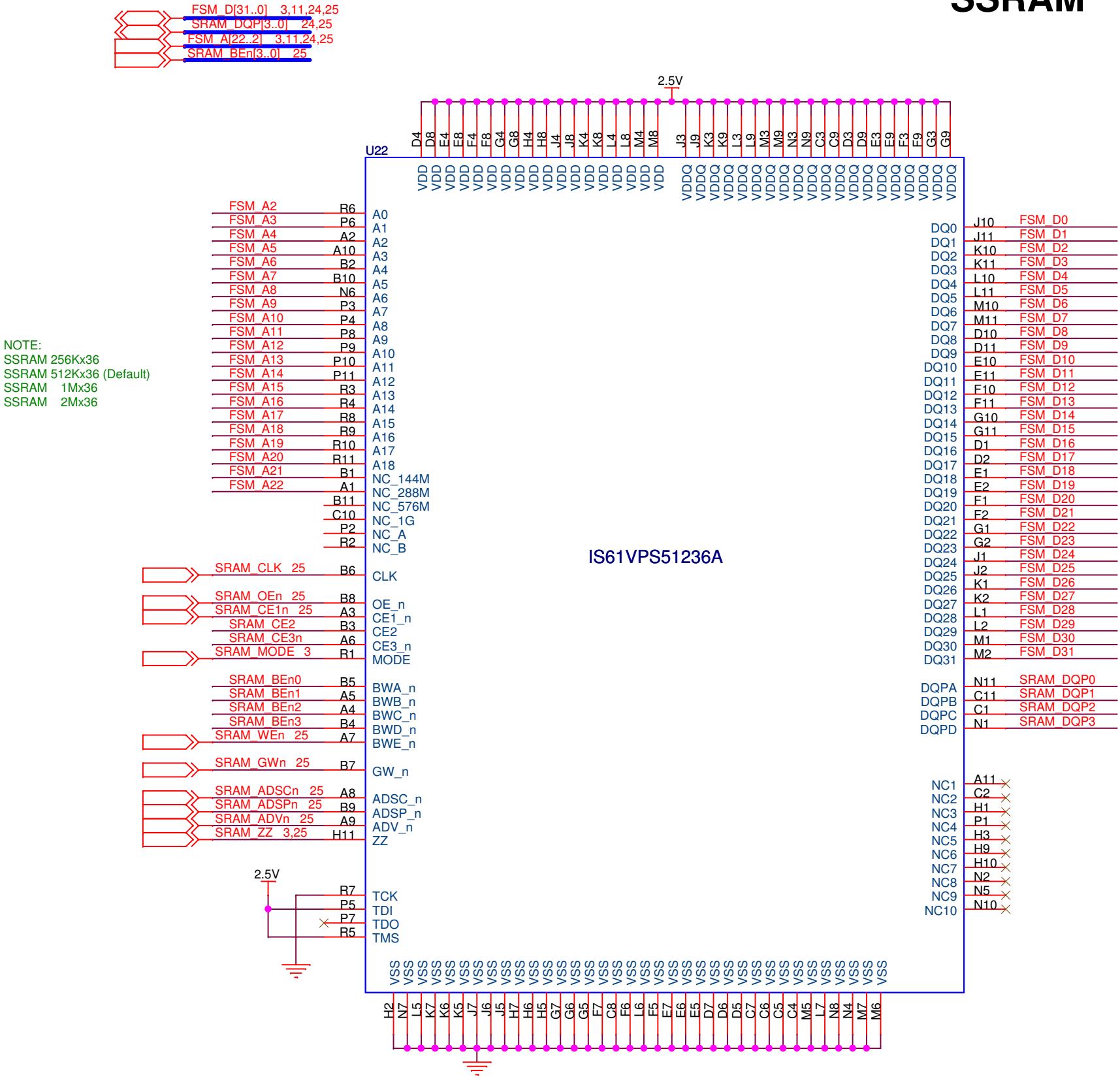
Place near the DDR2 SO-DIMM



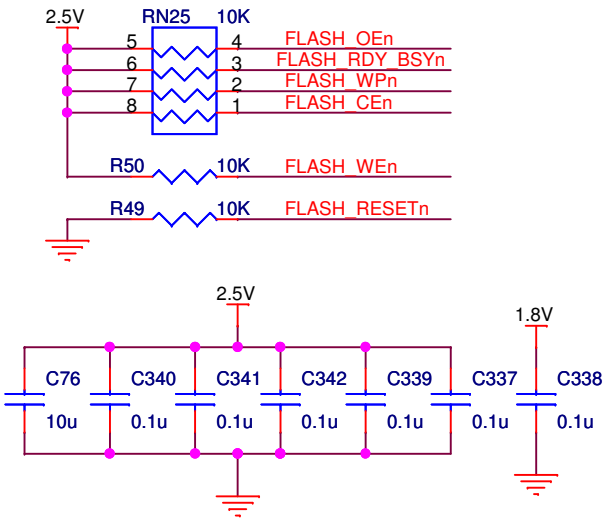
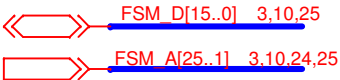
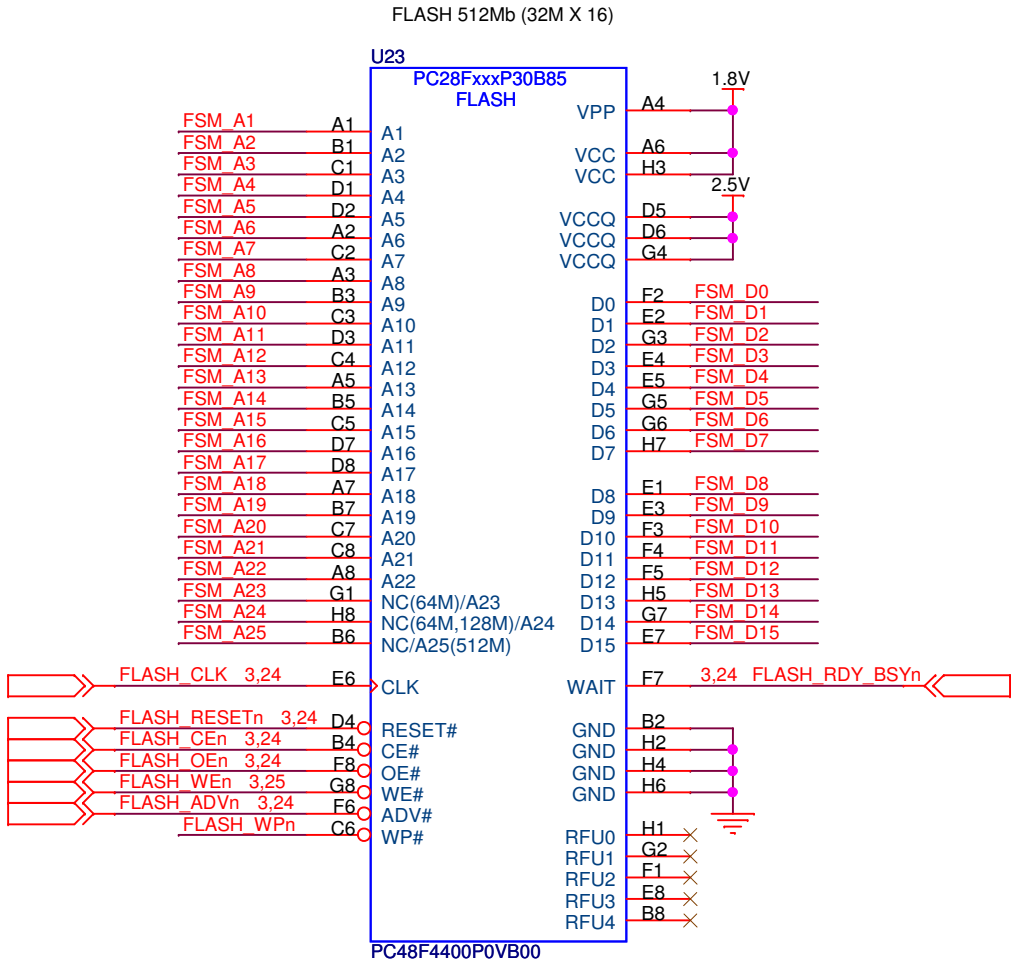
DDR3 Memory Device



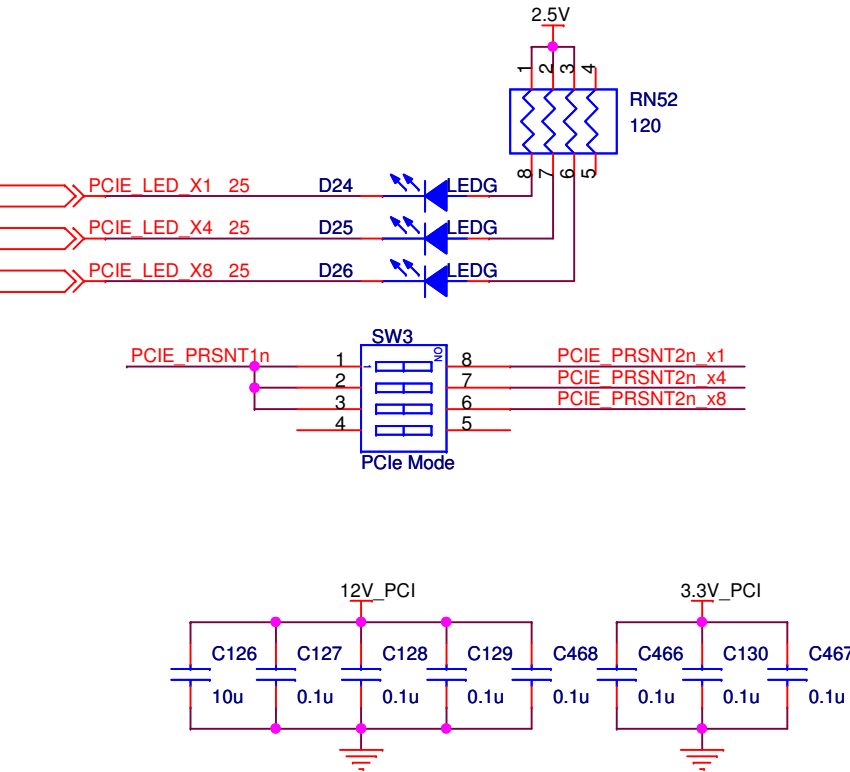
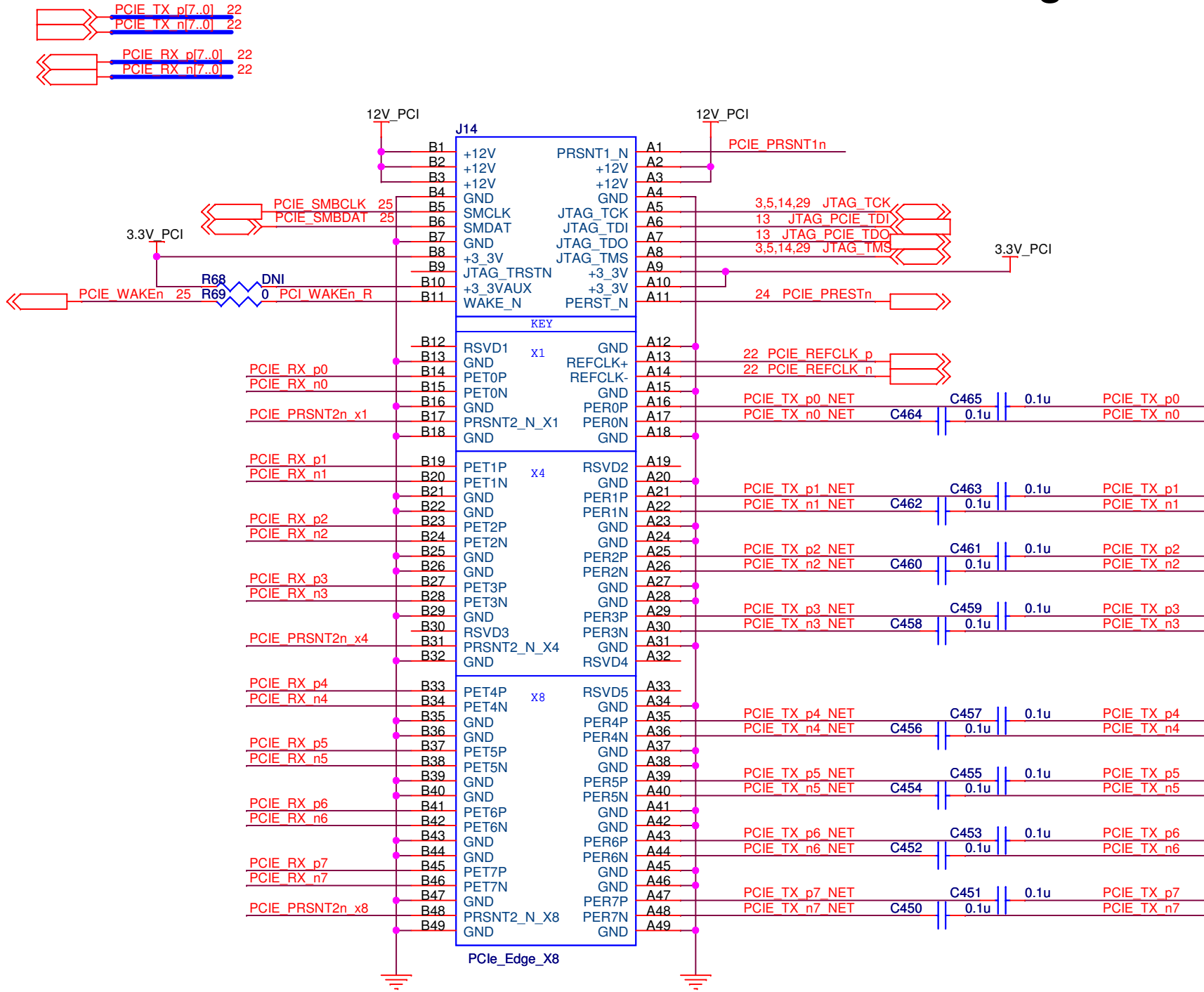
SSRAM



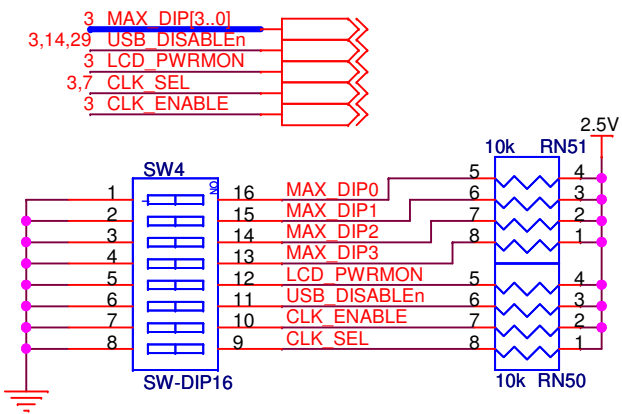
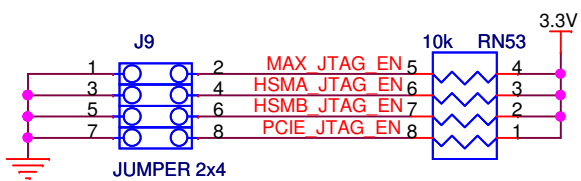
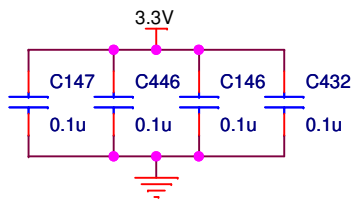
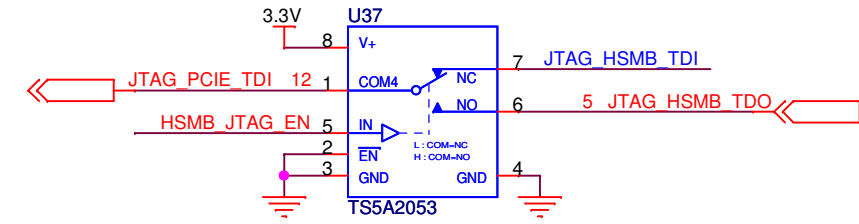
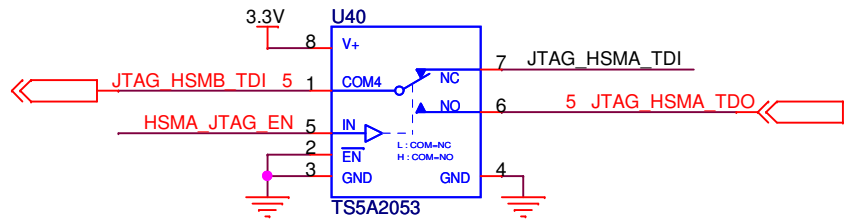
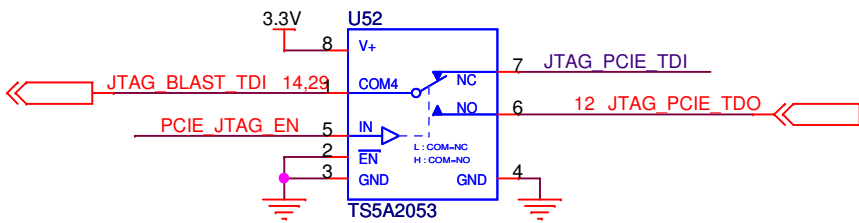
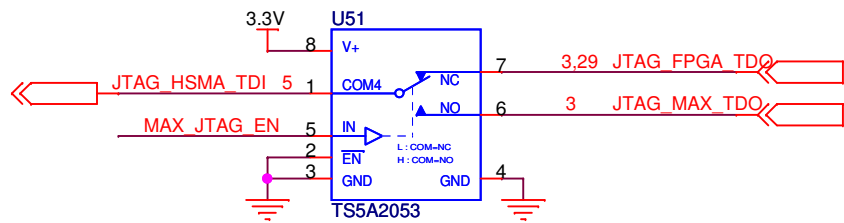
Sync Flash



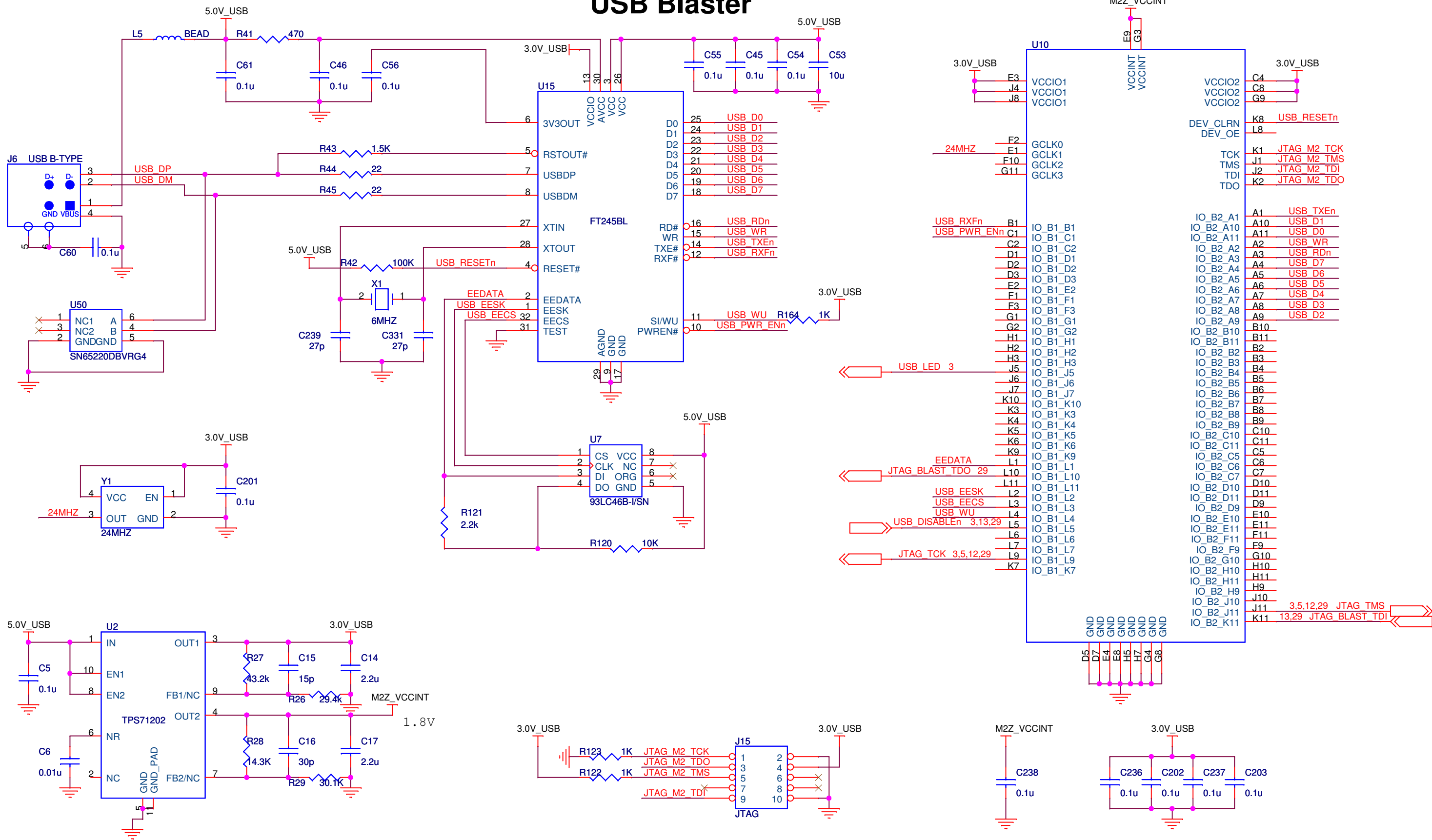
PCle x8 Edge Connector



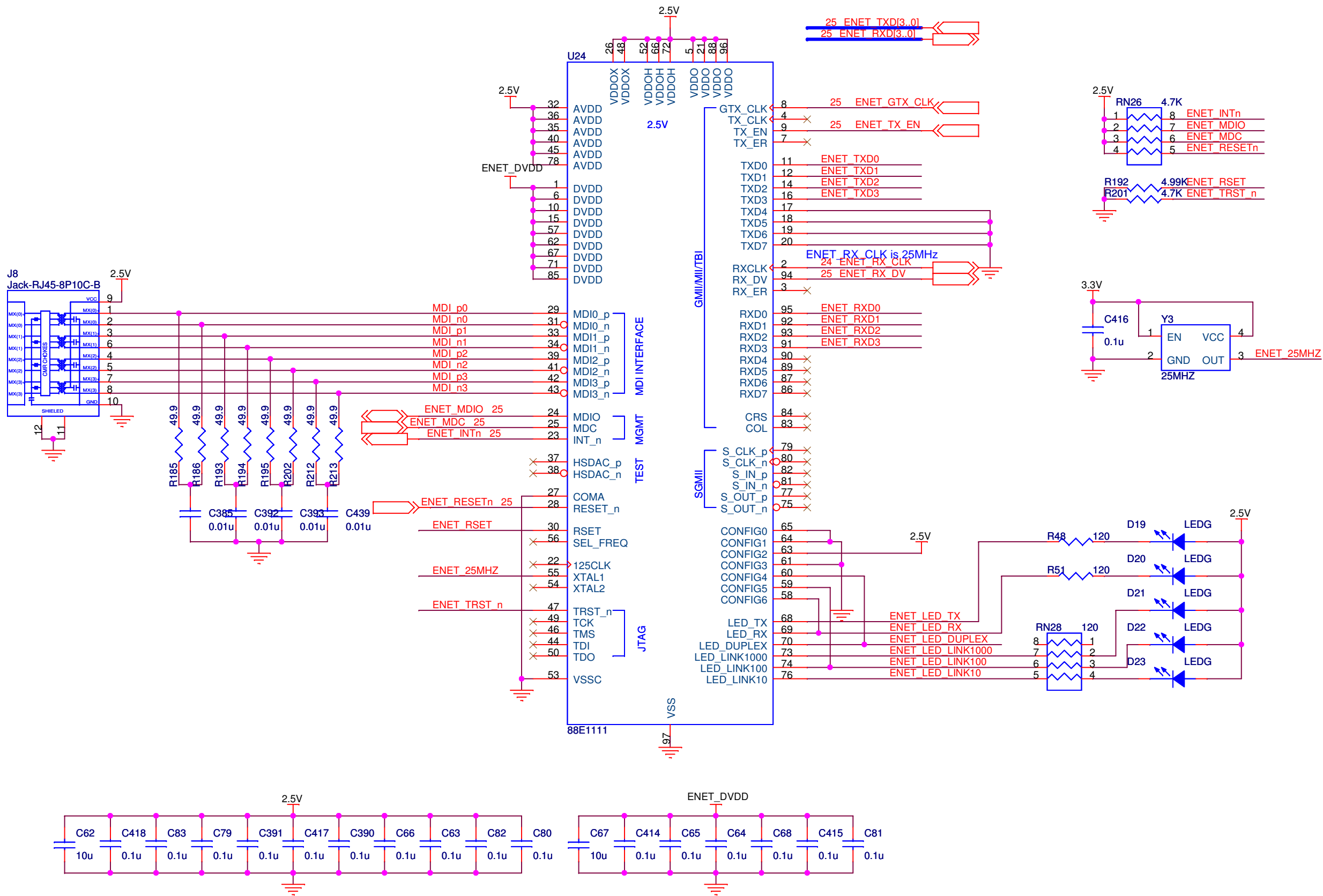
JTAG Control & Setting



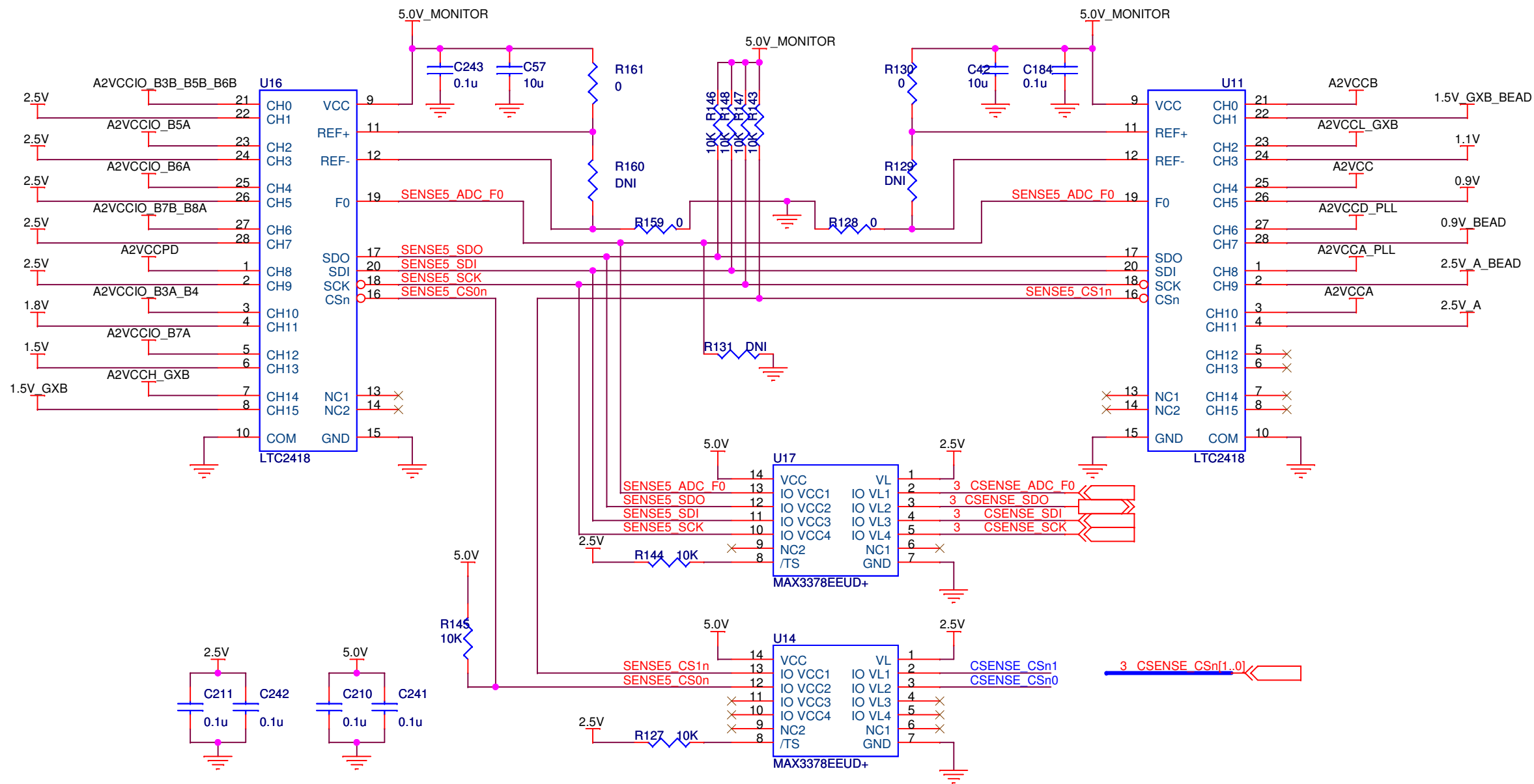
USB Blaster



Ethernet

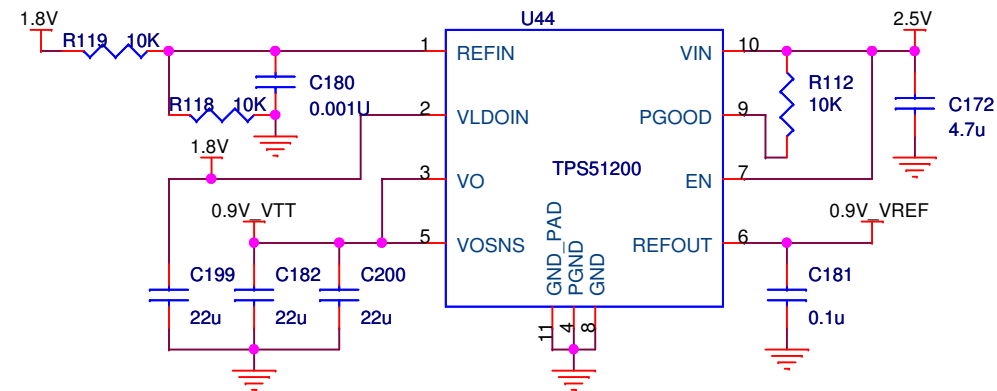


Power Monitor

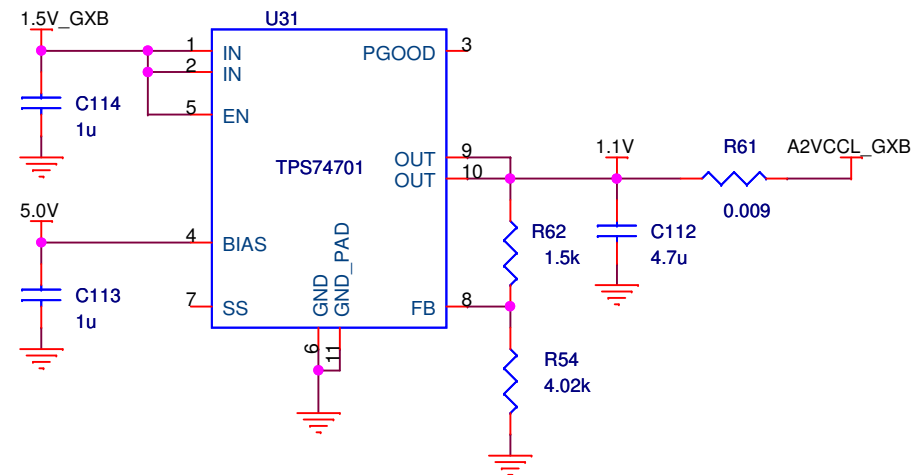


1.1V, 1.0V, VTT & VREF

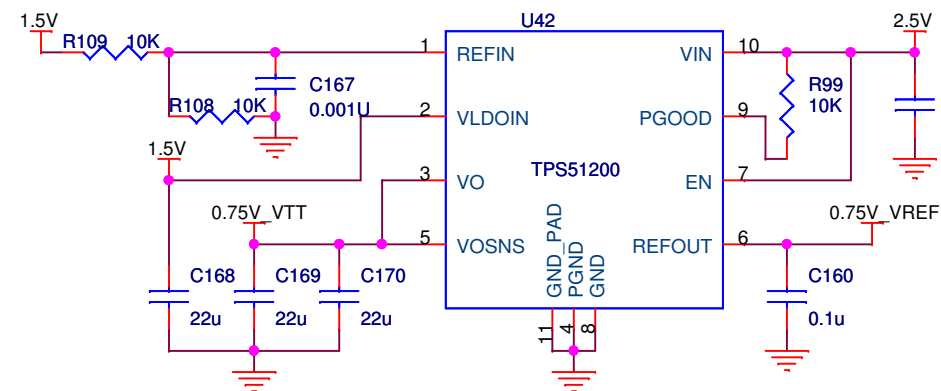
DDR2 VTT, VREF



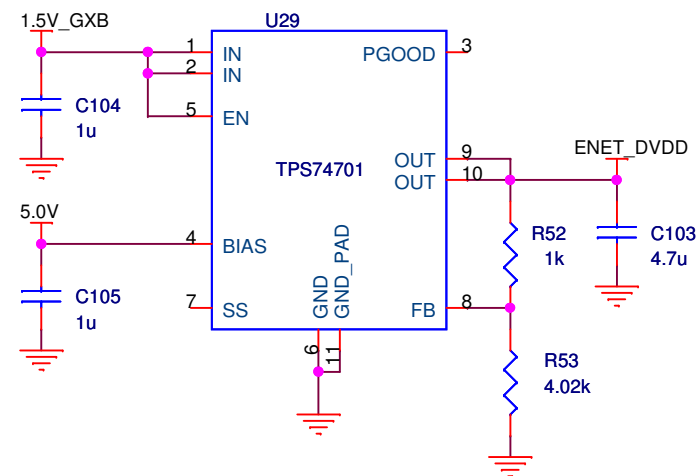
1.1V/500mA



DDR3 VTT, VREF



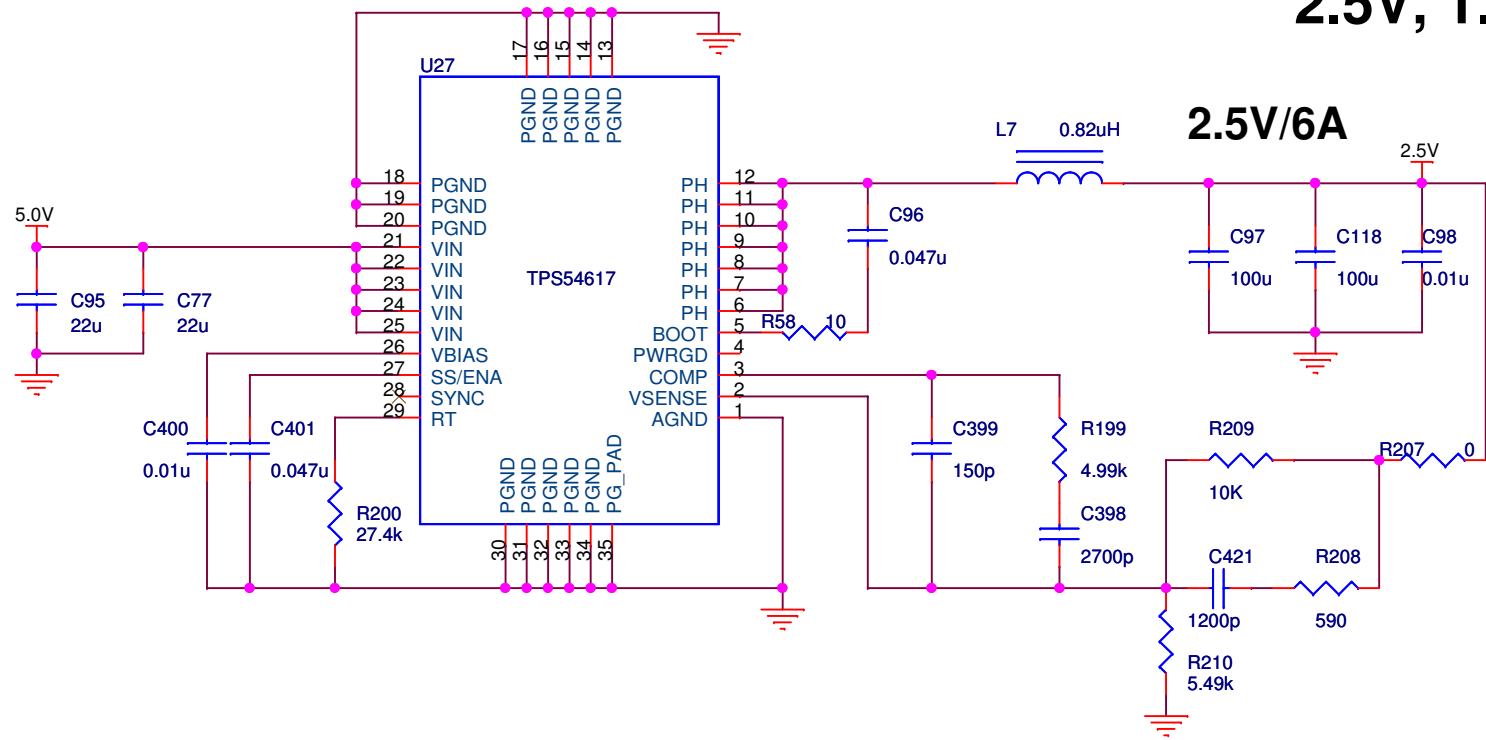
1.0V/500mA



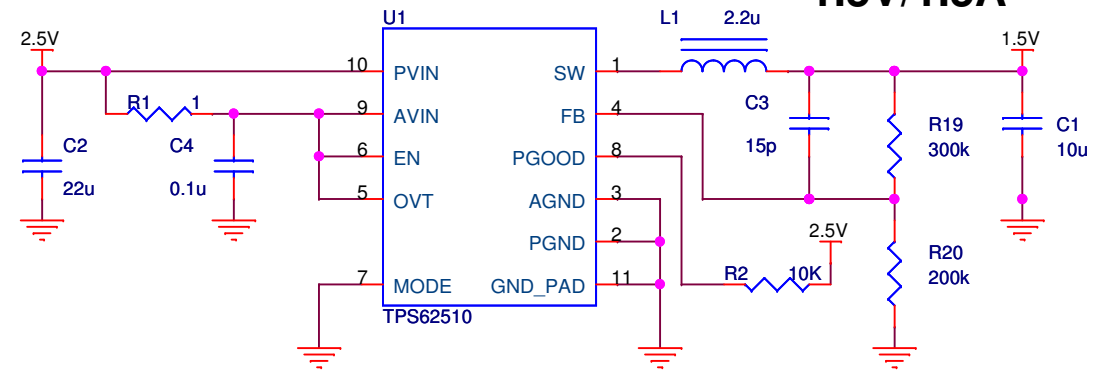
MTG1 MTG9 MTG5 MTG4 MTG3 MTG2 MTG7 MTG8 MTG6 MTG10
GND GND GND GND GND GND GND GND GND GND

FID6 FID8 FID7 FID9 FID10 FID4 FID3 FID2 FID1 FID5

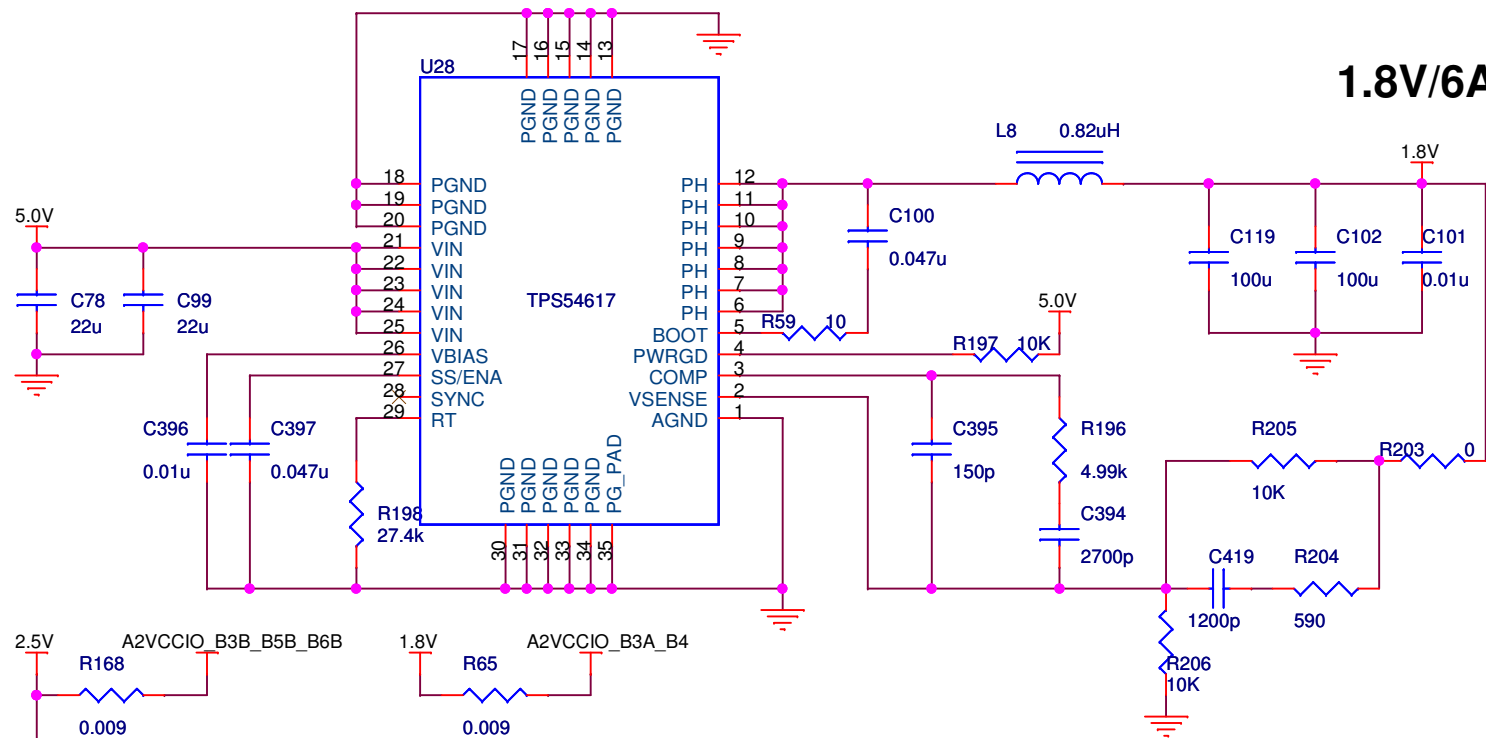
2.5V, 1.8V & 1.5V



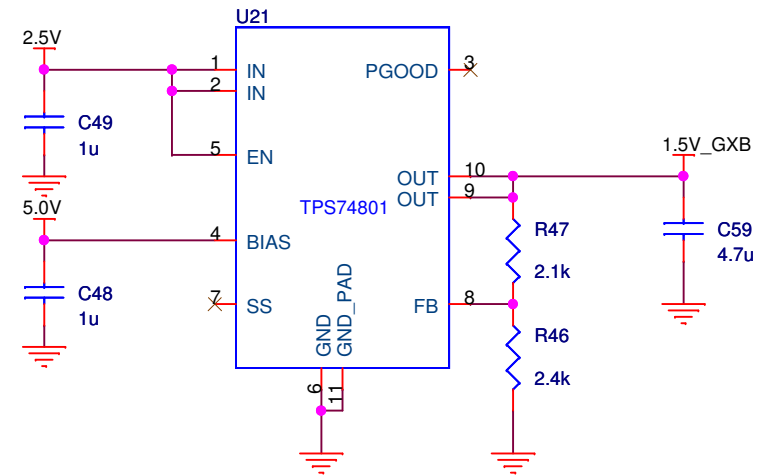
1.5V/1.5A



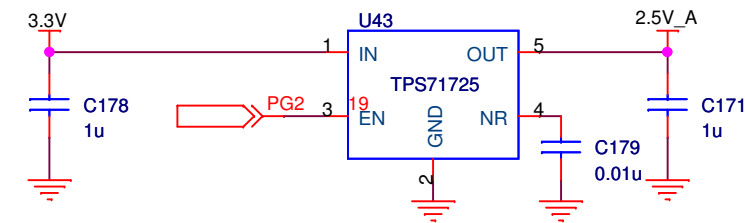
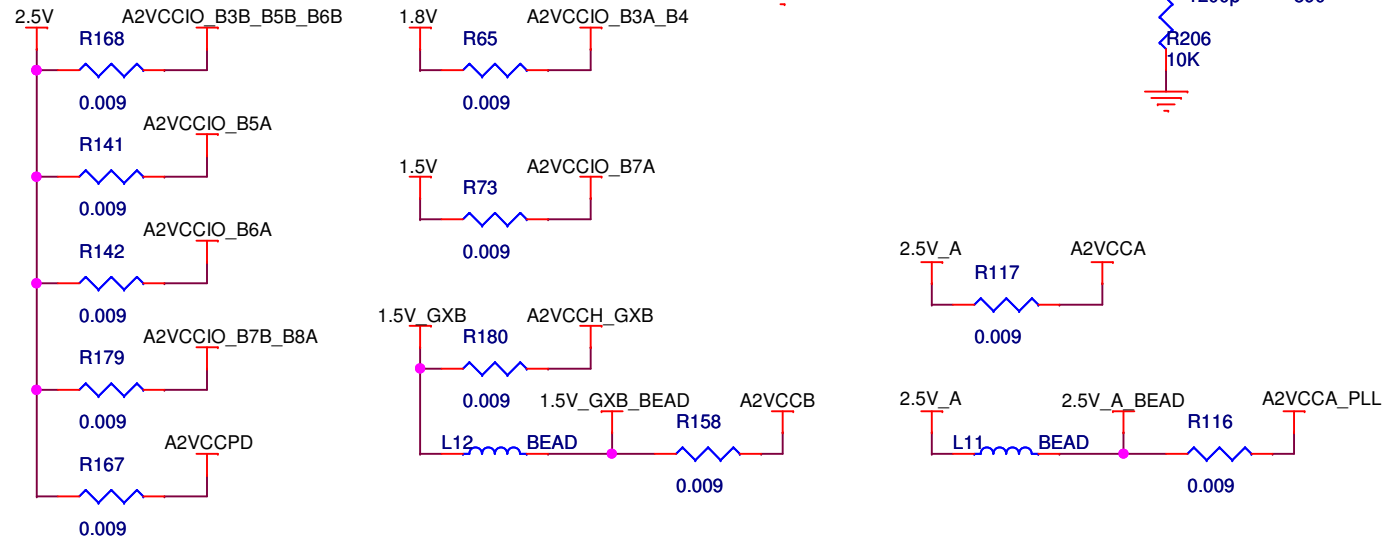
1.8V/6A



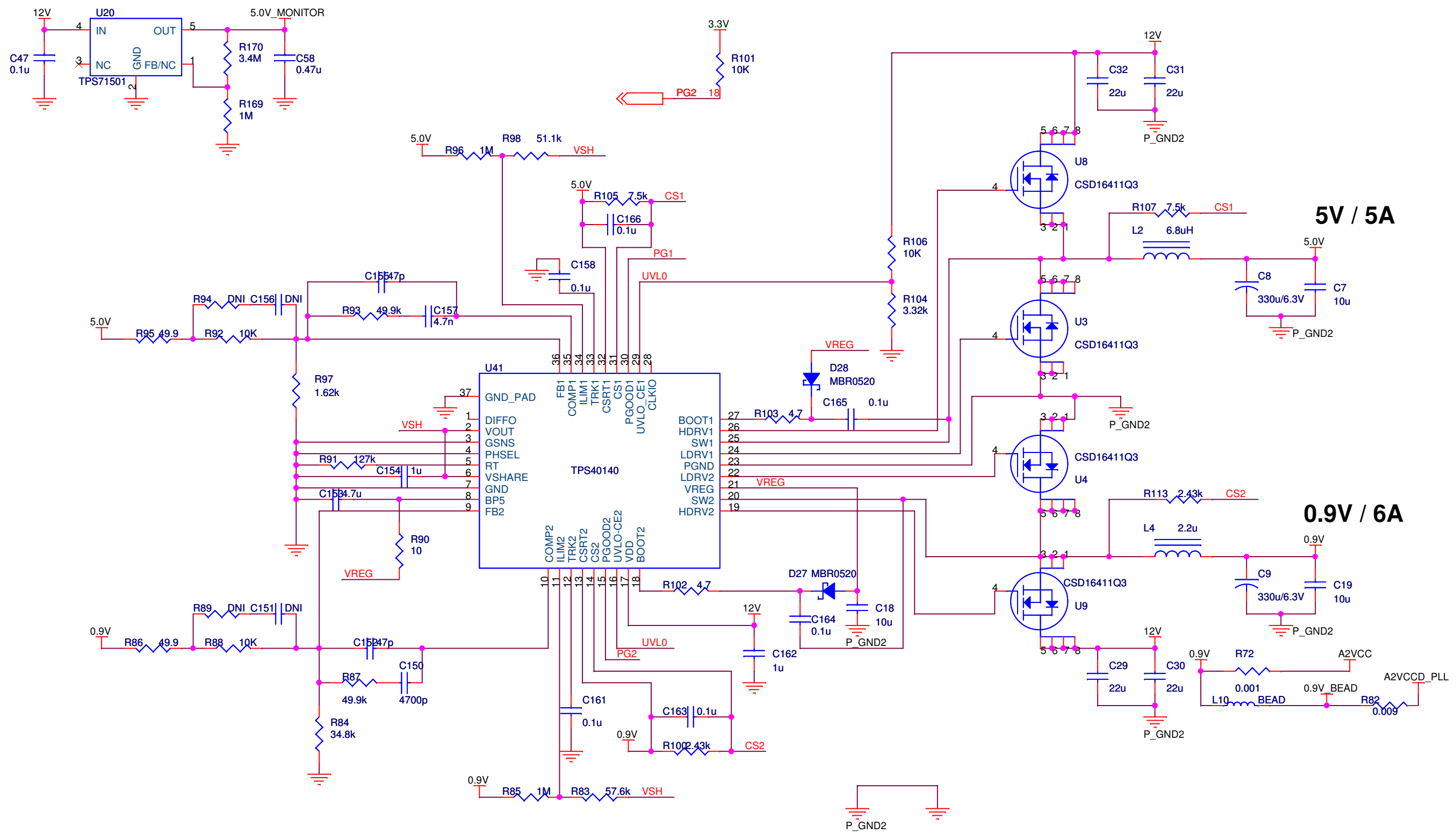
1.5V/1.5A



2.5V/150mA

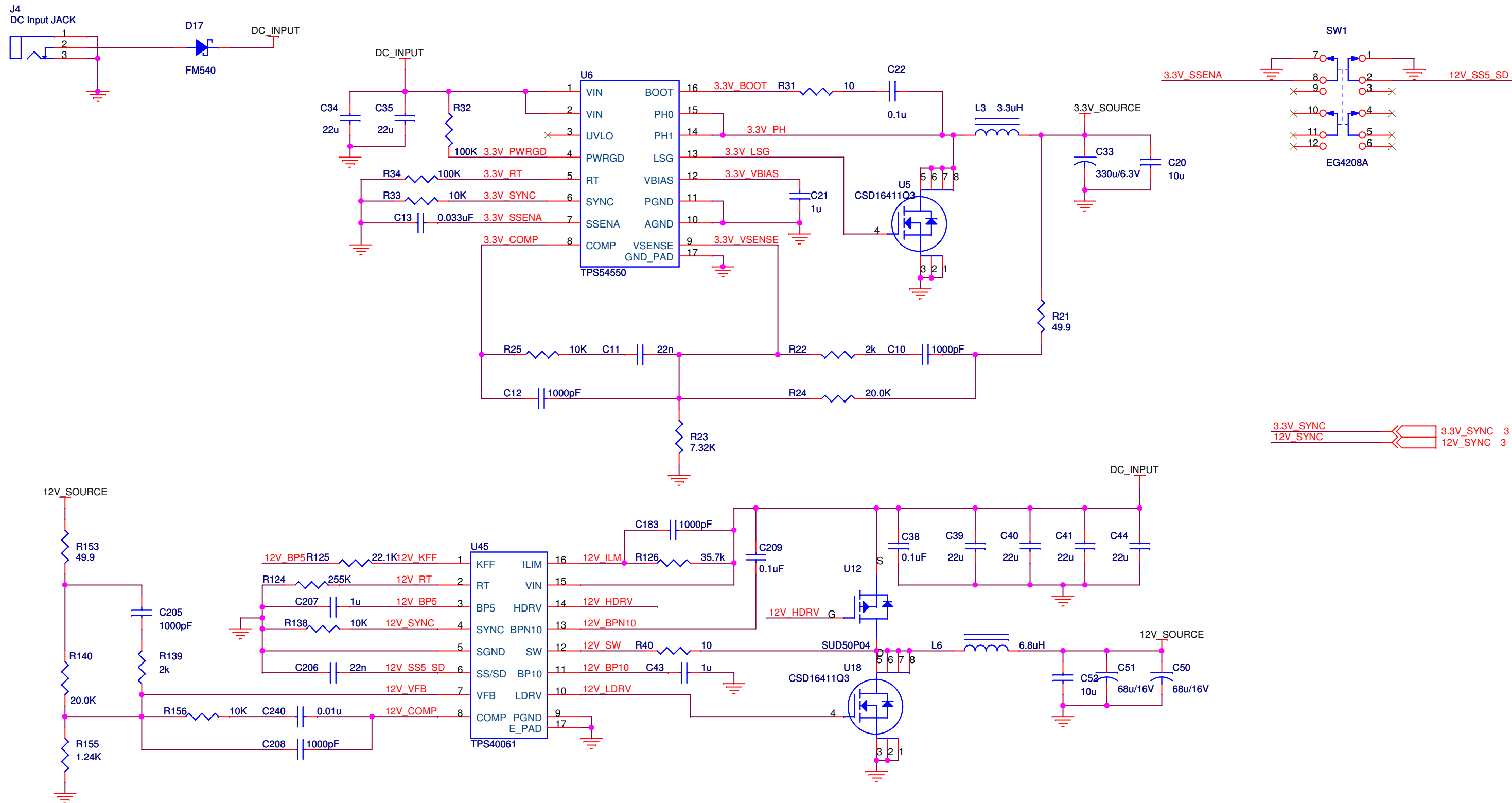


5V & 0.9V Dual Output



DC IN to 12V & 3.3V

14V ~ 20V DC Input



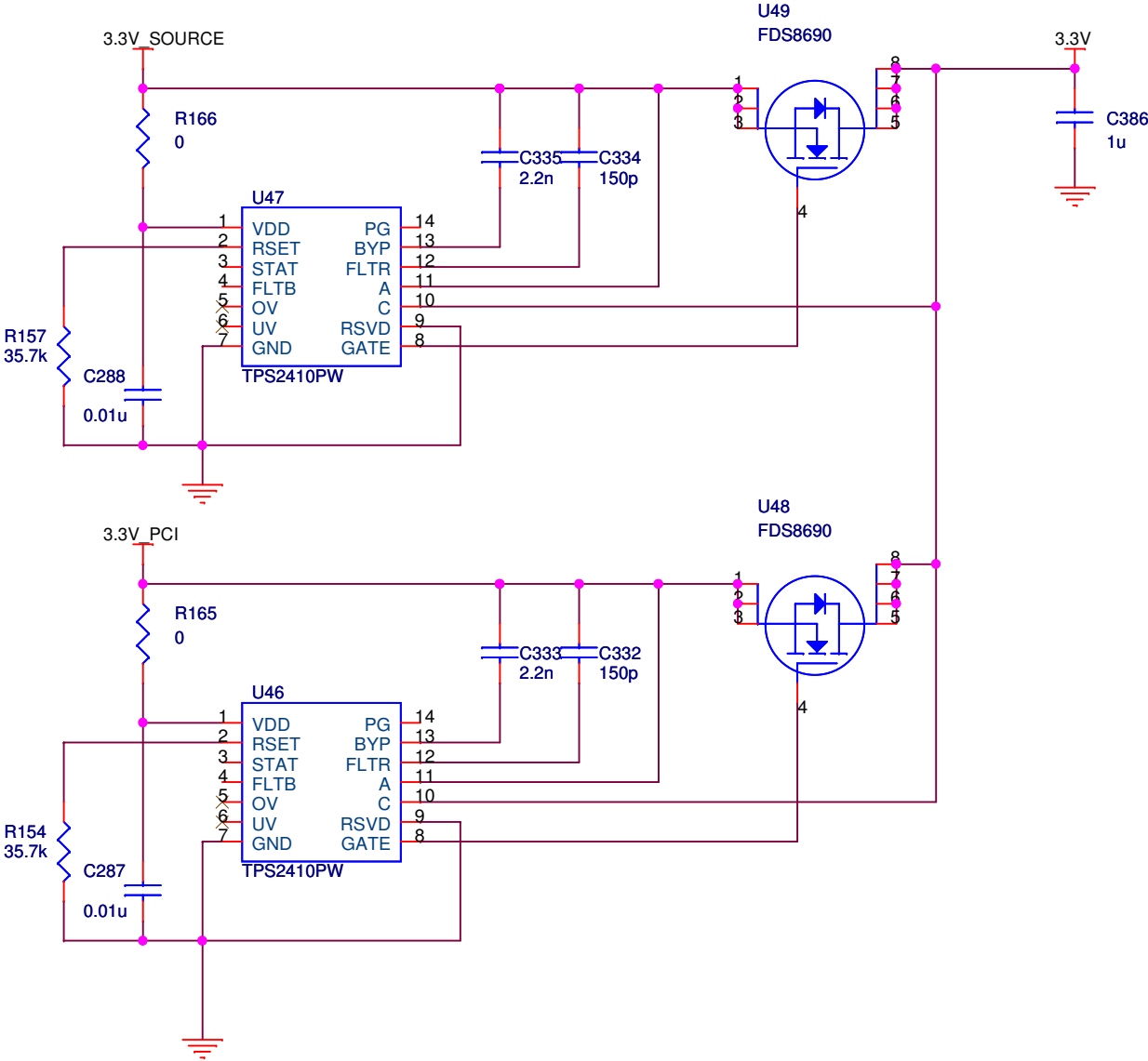
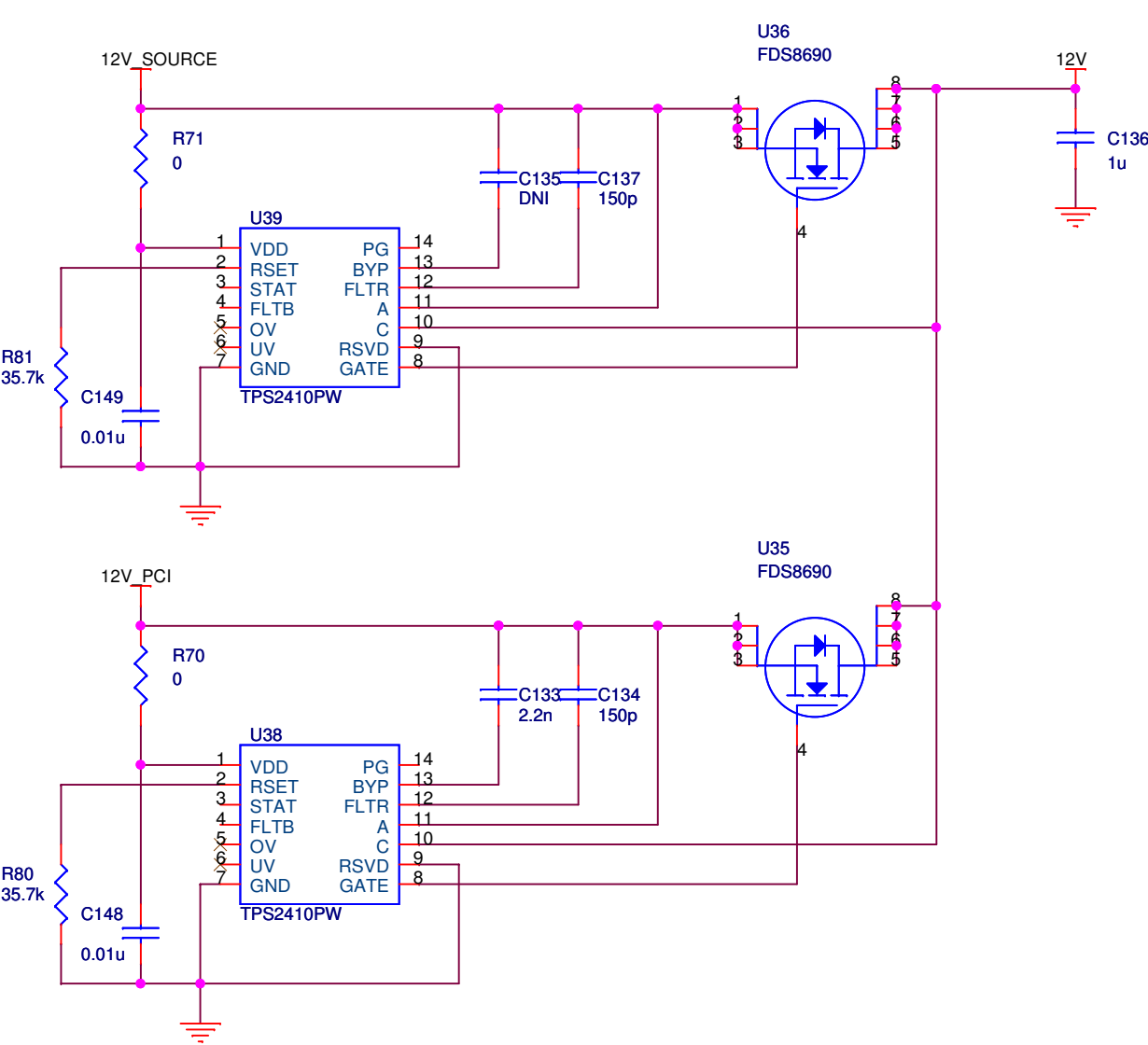
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Arria II GX FPGA Development Kit Board

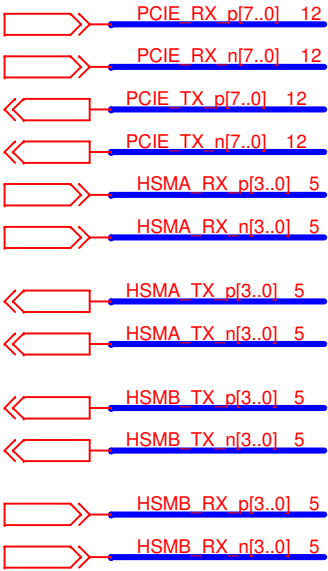
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Power MUX



BANK QL



PCIE_RX_p0	AN33
PCIE_RX_n0	AN34
PCIE_RX_p1	AL33
PCIE_RX_n1	AL34
PCIE_RX_p2	AJ33
PCIE_RX_n2	AJ34
PCIE_RX_p3	AG33
PCIE_RX_n3	AG34
PCIE_RX_p4	AE33
PCIE_RX_n4	AE34
PCIE_RX_p5	AC33
PCIE_RX_n5	AC34
PCIE_RX_p6	AA33
PCIE_RX_n6	AA34
PCIE_RX_p7	W33
PCIE_RX_n7	W34
HSMA_RX_p0	U33
HSMA_RX_n0	U34
HSMA_RX_p1	R33
HSMA_RX_n1	R34
HSMA_RX_p2	N33
HSMA_RX_n2	N34
HSMA_RX_p3	L33
HSMA_RX_n3	L34
HSMB_RX_p0	J33
HSMB_RX_n0	J34
HSMB_RX_p1	G33
HSMB_RX_n1	G34
HSMB_RX_p2	E33
HSMB_RX_n2	E34
HSMB_RX_p3	C33
HSMB_RX_n3	C34

U19A
Arria II GX Bank QL
EP2AGX260 (EP2AGX125)

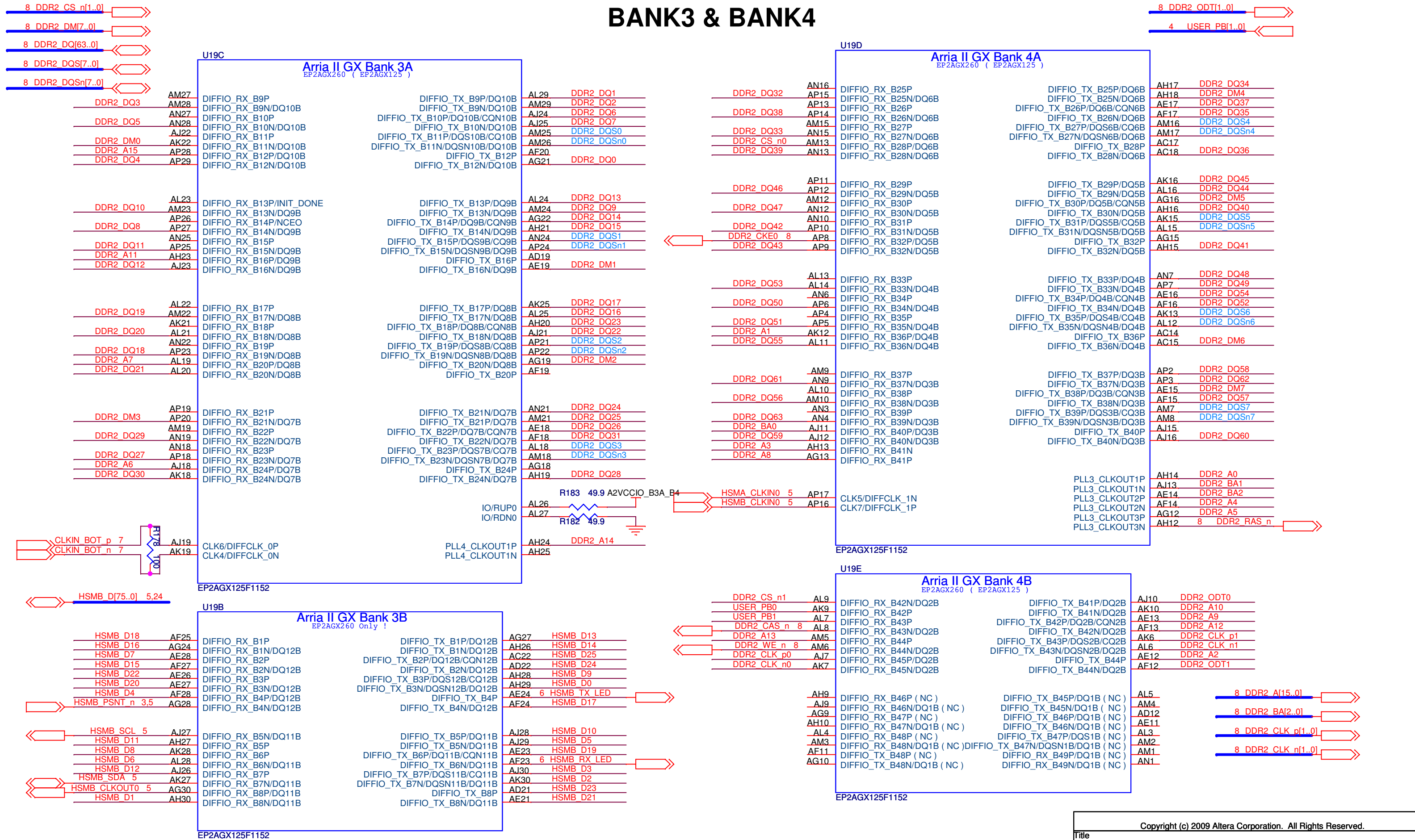
GXB_RX0P	GXB_TX0P	AM31	PCIE_TX_p0
GXB_RX0N	GXB_TX0N	AM32	PCIE_TX_n0
GXB_RX1P	GXB_TX1P	AK31	PCIE_TX_p1
GXB_RX1N	GXB_TX1N	AK32	PCIE_TX_n1
GXB_RX2P	GXB_TX2P	AH31	PCIE_TX_p2
GXB_RX2N	GXB_TX2N	AH32	PCIE_TX_n2
GXB_RX3P	GXB_TX3P	AF31	PCIE_TX_p3
GXB_RX3N	GXB_TX3N	AF32	PCIE_TX_n3
GXB_RX4P	GXB_TX4P	AD31	PCIE_TX_p4
GXB_RX4N	GXB_TX4N	AD32	PCIE_TX_n4
GXB_RX5P	GXB_TX5P	AB31	PCIE_TX_p5
GXB_RX5N	GXB_TX5N	AB32	PCIE_TX_n5
GXB_RX6P	GXB_TX6P	Y31	PCIE_TX_p6
GXB_RX6N	GXB_TX6N	Y32	PCIE_TX_n6
GXB_RX7P	GXB_TX7P	V31	PCIE_TX_p7
GXB_RX7N	GXB_TX7N	V32	PCIE_TX_n7
GXB_RX8P	GXB_TX8P	T31	HSMA_TX_p0
GXB_RX8N	GXB_TX8N	T32	HSMA_TX_n0
GXB_RX9P	GXB_TX9P	P31	HSMA_TX_p1
GXB_RX9N	GXB_TX9N	P32	HSMA_TX_n1
GXB_RX10P	GXB_TX10P	M31	HSMA_TX_p2
GXB_RX10N	GXB_TX10N	M32	HSMA_TX_n2
GXB_RX11P	GXB_TX11P	K31	HSMA_TX_p3
GXB_RX11N	GXB_TX11N	K32	HSMA_TX_n3
GXB_RX12P (NC)	GXB_TX12P (NC)	H31	HSMB_TX_p0
GXB_RX12N (NC)	GXB_TX12N (NC)	H32	HSMB_TX_n0
GXB_RX13P (NC)	GXB_TX13P (NC)	F31	HSMB_TX_p1
GXB_RX13N (NC)	GXB_TX13N (NC)	F32	HSMB_TX_n1
GXB_RX14P (NC)	GXB_TX14P (NC)	D31	HSMB_TX_p2
GXB_RX14N (NC)	GXB_TX14N (NC)	D32	HSMB_TX_n2
GXB_RX15P (NC)	GXB_TX15P (NC)	B31	HSMB_TX_p3
GXB_RX15N (NC)	GXB_TX15N (NC)	B32	HSMB_TX_n3

PCIE_REFCLK_p_12	AE29	REFCLK0P
PCIE_REFCLK_n_12	AE30	REFCLK0N
CLKIN_REF_Q1_1_p_7	AA29	REFCLK1P
CLKIN_REF_Q1_1_n_7	AA30	REFCLK1N
CLKIN_REF_Q2_p_7	U29	REFCLK2P
CLKIN_REF_Q2_n_7	U30	REFCLK2N
CLKIN_REF_Q3_p_7	N29	REFCLK3P (NC)
CLKIN_REF_Q3_n_7	N30	REFCLK3N (NC)
	AC29	REFCLK4P
	AC30	REFCLK4N
CLKIN_REF_Q1_2_p_7	W29	REFCLK5P
CLKIN_REF_Q1_2_n_7	W30	REFCLK5N
CLKIN_155_p_7	R29	REFCLK6P
CLKIN_155_n_7	R30	REFCLK6N
	L29	REFCLK7P (NC)
	L30	REFCLK7N (NC)

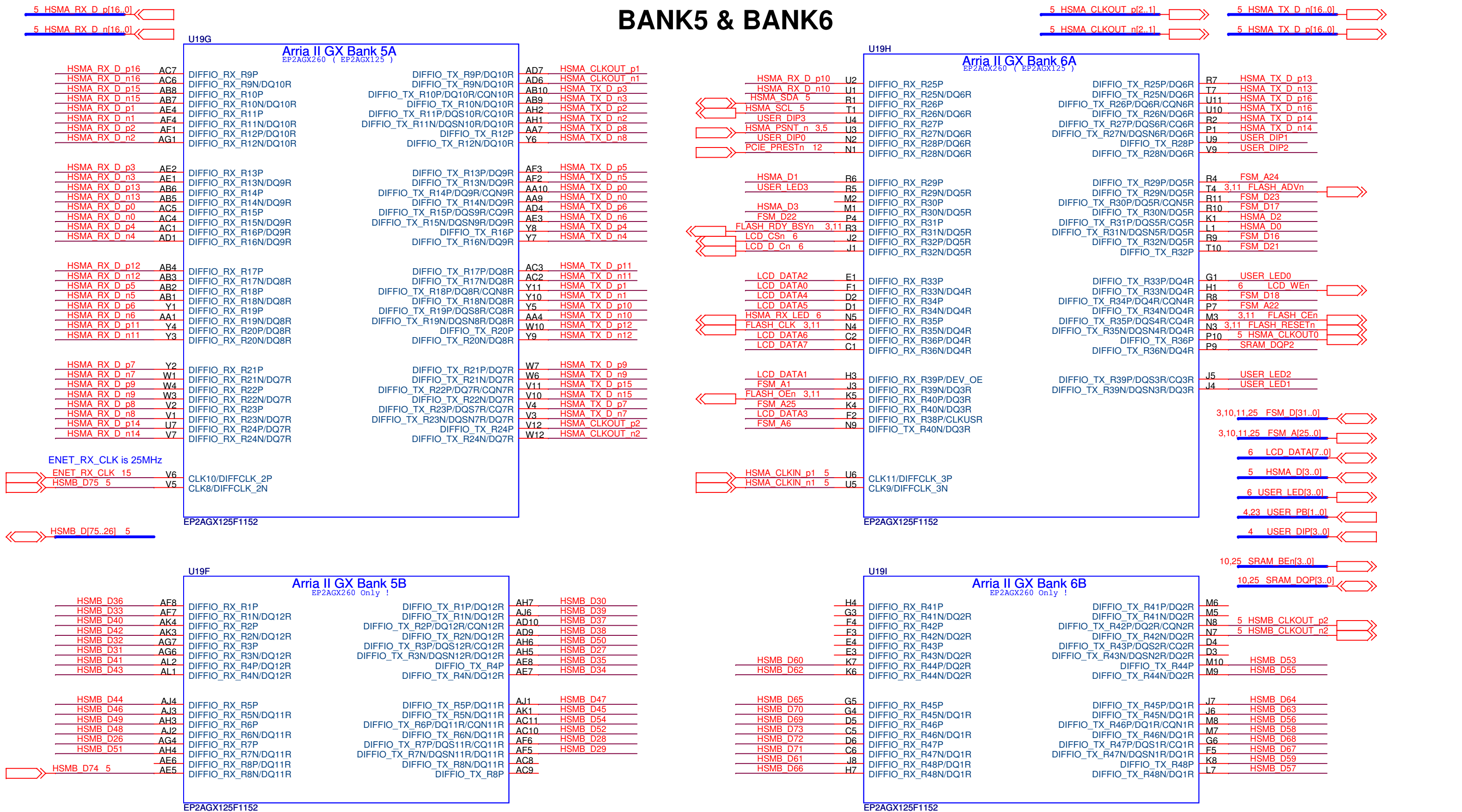
EP2AGX125F1152

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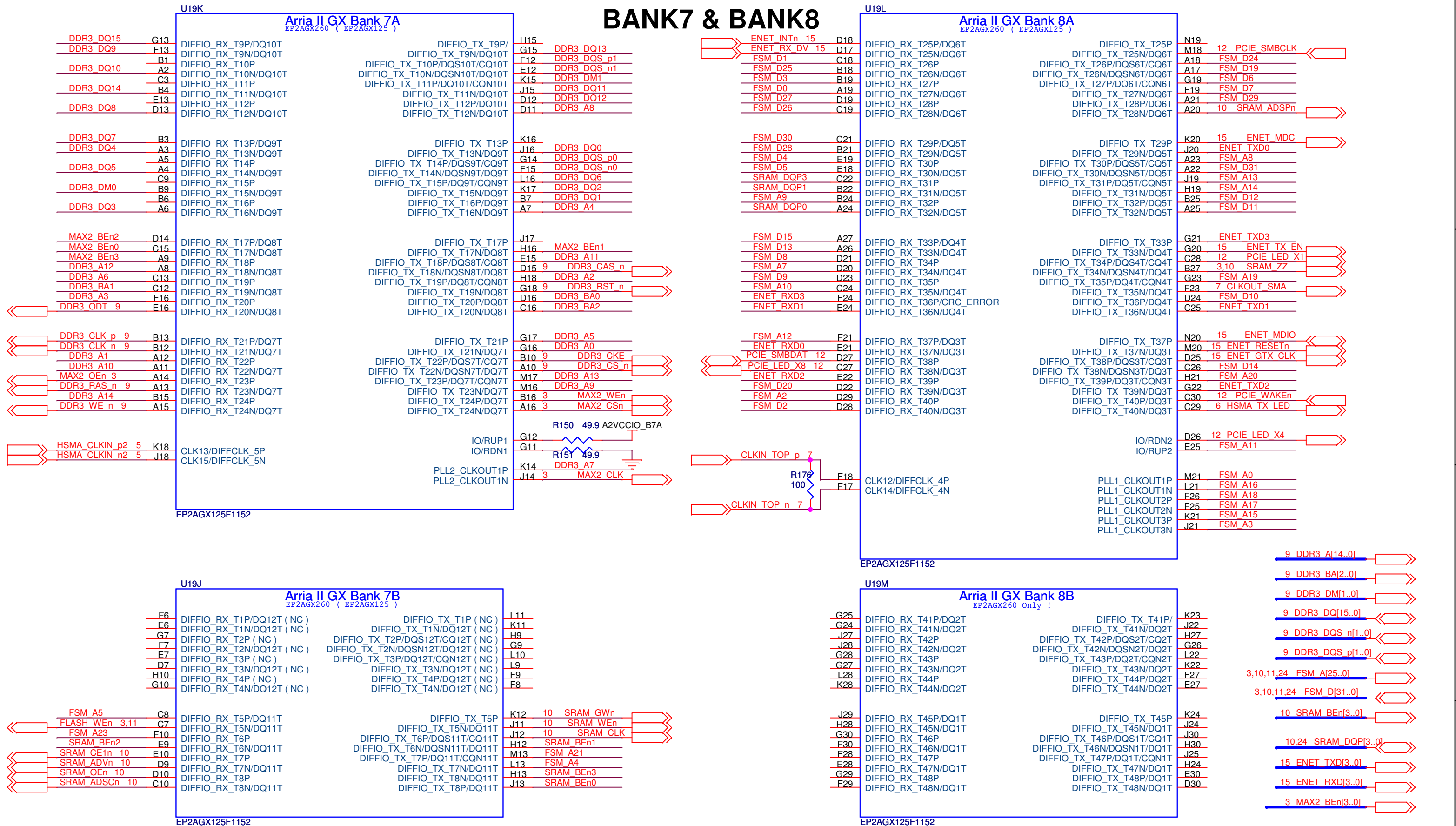
BANK3 & BANK4



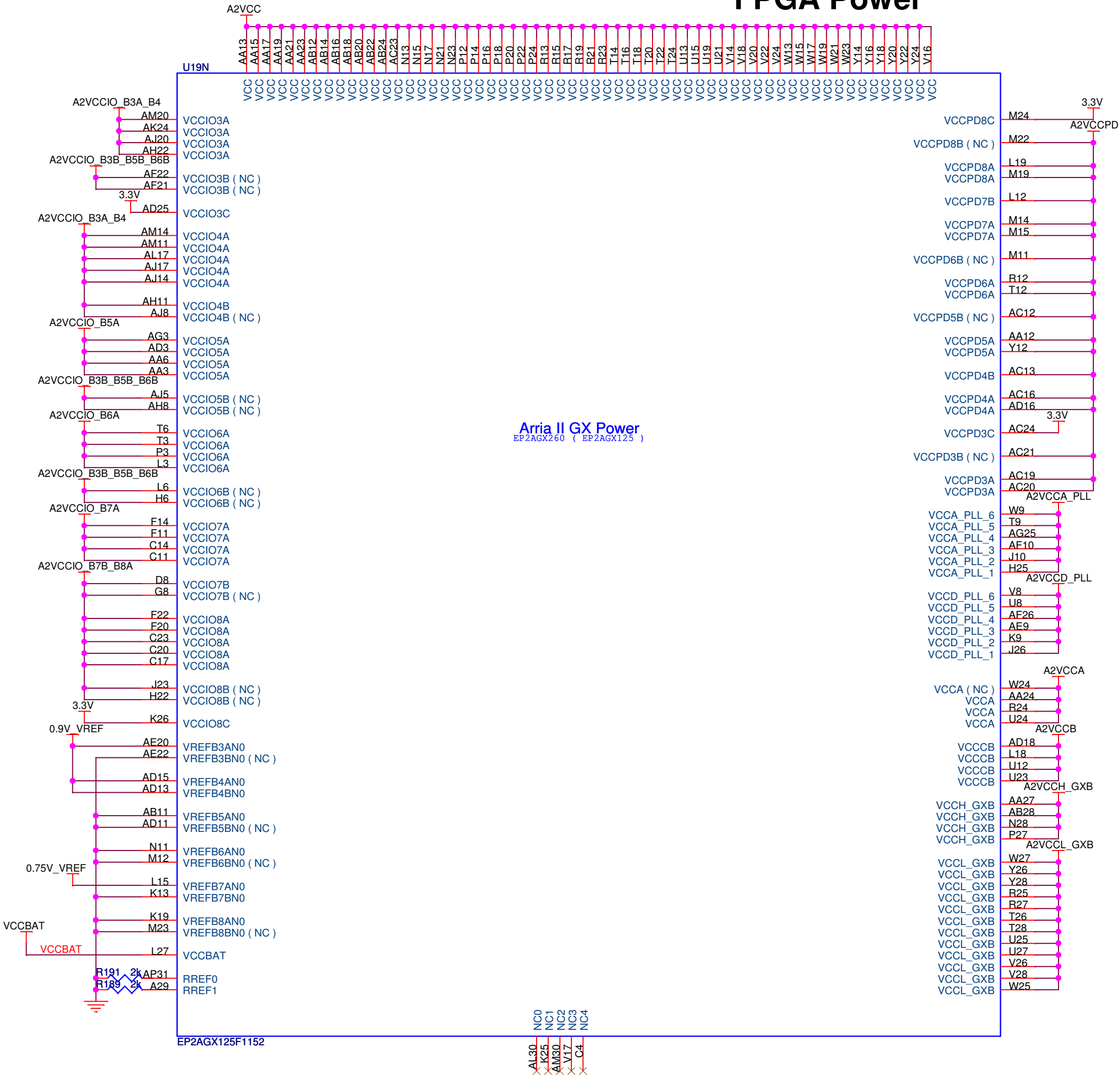
BANK5 & BANK6



BANK7 & BANK8



FPGA Power

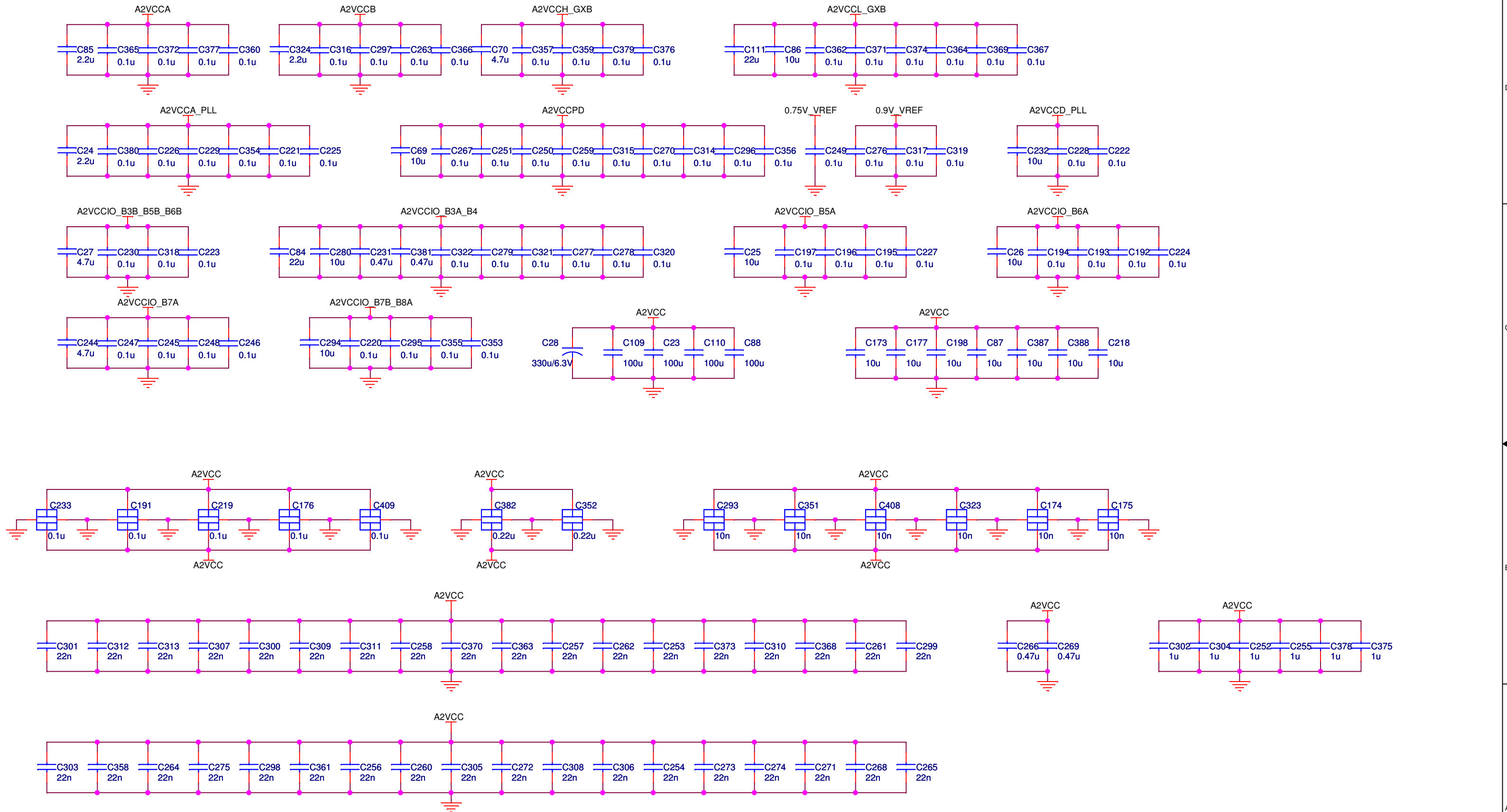


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FPGA Ground



FPGA Decoupling



FPGA Configuration

