

This project has been passed to P.E.R.C. where it is now in Mentor's formats.

50MHz
VCTCXO

3.5GHz Clock

DDS

FPGA

Altera
MAX 10
IC1
10M08SAE144I7G

Not sure which

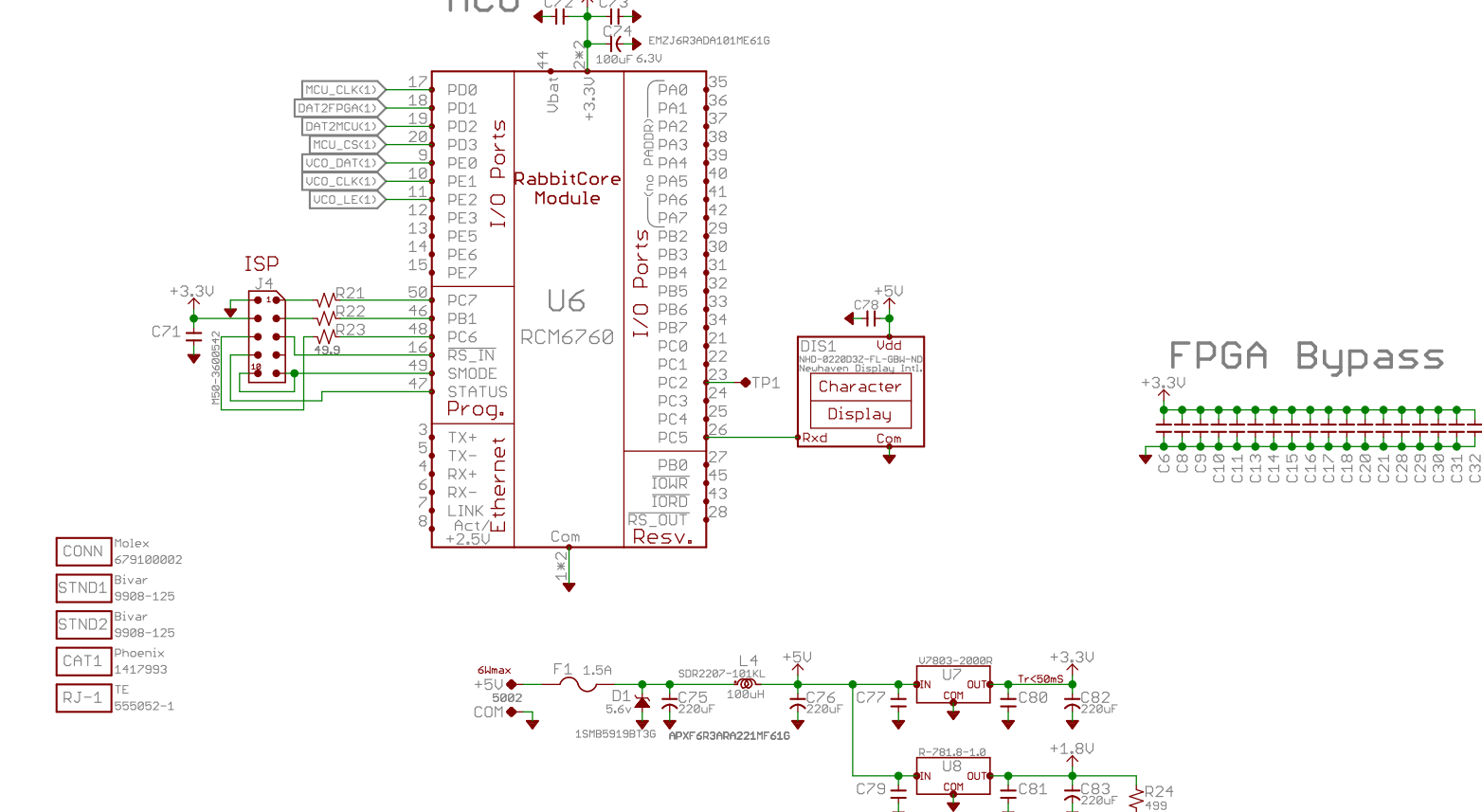
HSNK1 U2017B
HSNK2 XL198-10-2.25-P

NOTES:

- 1) All caps 0.1uF X7R unless otherwise mentioned.
- 2) Are 50 Ohm pullups on DDS output necessary? Datasheet says no, eval board has them.

Ltr	Date	By	REVISION DESCRIPTION	
University of Toronto, Quantum Optics Group				
Design: A.Stummer			High Nyquist DDS Amar Vutha Labs	
Date: 2016 March				
Edited: 30-Mar-16 9:49 AM				
File: Nyquie Plus			Sheet: 1 of 2	REV: A

A	B	C	D
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University of Toronto
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High Nyquist DDS