Single Active Element PID Controllers

Vratislav MICHAL [1,2], *Christophe PRÉMONT* [2], *Gaël PILLONNET* [1], *Nacer ABOUCHI* [1]

[1] CPE-Lyon, 43, boulevard du 11 Novembre 1918, Villeurbanne, France
[2] ST-Ericsson, 12 rue Jules Horowitz, Grenoble, France

vratislav.michal@cpe.fr, www.postreh.com/vmichal

Abstract. *This paper presents a detailed overview of the circuits allowing the realization of PID controllers with single active element. We provide analysis of the circuits using the operational amplifier (OpAmp) and operational transconductance amplifiers (OTA). Based on these analyses, we present an alternative structure using the second generation current conveyer CCII. Compared to the classical solutions, presented controller exhibits improved features such as symmetrical transfers of feedback and reference paths. The paper is completed by the design equations and the example of design.*

Keywords

Analog PID controller, CCII-based PID, OTA-based PID, OpAmp-based PID, DC - DC converter control.

1. Introduction

Classical implementations of the PID controller contain several active elements to realize the transfer function. For instance, parallel structure using operational amplifiers (OpAmp) [1] requires five amplifiers: differential input amplifier, P, I, D transfers and adder. Some recent work presents the PID controllers in voltage or current mode with alternative building blocks. For instance [2], [3], [4] show the PID controllers based on CCII current conveyors, OTA or CDTA, respectively. All these circuits allow independent tuning of P, I and D components, however, despite the high circuit complexity and power consumption. These parameters can affect the power efficiency, cost, as well as the competitiveness of the analog control to their discrete-time counterparts.

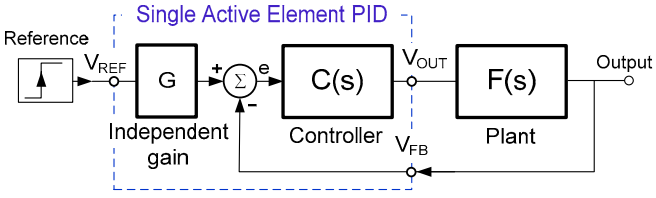

Fig. 1. Structure of SISO closed-loop system with single active element PID controller C(s).

Compared to these solutions, utilization of single active element controllers (see *e.g.* [4] or [5] for OpAmp and OTA) offer a very cost-effective solution for many applications, such as the smart portable devices. The controller with single active element is depicted on the block scheme of a SISO system in Fig. 1. We notice that the controller include following functions:

- *Differential block*
- *Transfer function of PID controller*
- *Independent gain G to adjust the reference input*
- *Symmetrical transfers* $|V_{OUT}/V_{REF}| = G \cdot |V_{OUT}/V_{FB}|$

In this article, we introduce the transfers of basic PID controllers in *section 2*. *Section 3* and *4* present standard single operational amplifier and OTA-based controllers. Here, some specific characteristics are highlighted. Namely the asymmetrical transfers of $|V_{OUT}/V_{REF}|$ and $|V_{OUT}/V_{FB}|$ and realization of independent gain *G*. In the last *section 5*, an alternative structure using the CCII current conveyor will be presented, competed by the design recommendation and application example.

2. Basic of the PID controller

The controller transfer function can be defined in many different ways [7]. From the electrical point of view, we focus mainly on the transfer function numerator (*n*) and denominator (*d*) orders. As shown in Fig. 2, the ideal PID controller has two numerator zeros and one pole in the origin of the complex plane. Its high frequency gain increases to infinity. On this account, the ideal PID is unrealizable (non-causal). Therefore, we use a controller with derivative filtering, having identical numerator and denominator orders. This controller can be written in the transfer function form (1):

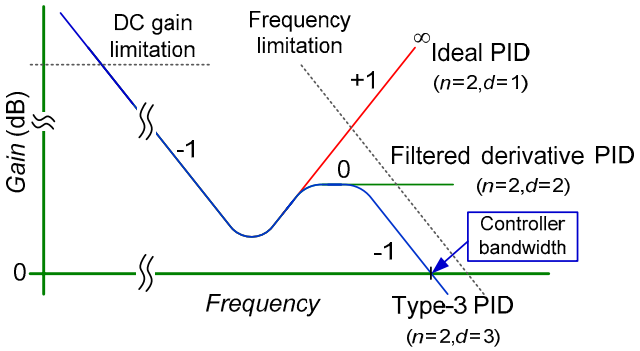

Fig. 2. Frequency transfers with indicated slopes of ideal, filtered derivative and type-3 PID controller.

$$C(s) = k\left(1 + \frac{1}{T_i s} + \frac{T_d s}{\alpha T_d s + 1}\right) \quad (1)$$

where T_i and T_d are the integrator and differentiator time constants, k is the gain and α the filtering factor [8]. However, Fig. 2 shows that derivative filtered controller (1) has ideally infinite frequency bandwidth, limited in reality by the active element (OpAmp) frequency range. This limitation is inaccurate and can results in some unpredictable behavior. In applications as the switched DC/DC converters (see [6]), the accurate control of the high frequency gain is obtained by an additional 1st order lag transfer $1/(s/p_2+1)$. Thus, all Fig. 2 controllers can be written in general zero-pole form (rad/s):

$$C(s) = K\frac{(s/z_1+1)(s/z_2+1)}{s\cdot(s/p_1+1)(s/p_2+1)} \quad (2)$$

where $p_1 = p_2 = \infty$ corresponds to the ideal PID, $p_1 < \infty$, $p_2 = \infty$ to the derivative filtered (or type-2) controller (1) and $p_1, p_2 < \infty$ to controller with additional first-order lag (referred as type-3 controller) – see example in section 5.2. Conversion between the controller forms (1) and (2) can be done by solving ordinary quadratic equations.

3. OA-based PID Controller

The most commonly used structure of PID controller is shown in Fig. 3. It contains one low impedance inverting input (V_{FB}), high impedance reference input (V_{REF}) and low impedance output V_{OUT}. The circuit can realize ideally all three described controllers (see example in section 5.2). Practical applications use derivative filtered (1) or type-3 controllers. The independent gain $G > 1$ is realized by optional resistance $R_4 = R_1/(G-1)$. Otherwise, $G = 1$.

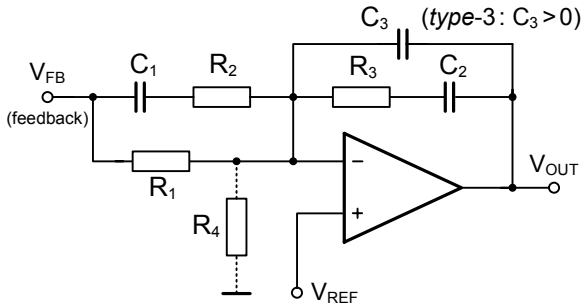

Fig. 3. OpAmp based Controller. R_4 is optional resistance related to G.

3.1 Circuit Analysis

The transfer function V_{OUT}/V_{FB} can be found as:

$$\frac{V_{OUT}}{V_{FB}} = \frac{-1}{R_1(C_2+C_3)}\frac{(R_3C_2s+1)(C_1(R_2+R_1)s+1)}{s(R_2C_1s+1)\left(\frac{C_2C_3}{C_2+C_3}R_3s+1\right)} \quad (3)$$

and corresponds directly to the transfer function $C(s)$ in Fig. 1 model. For type-3 transfer, the component values can be determined from zero/poles values p_1, p_2 and z_1, z_2 (rad/s), by comparing the coefficients of (2) and (3) as:

$$R_1 = r_1 \qquad R_2 = \frac{R_1 z_2}{p_1 - z_2} \qquad R_3 = \frac{R_1 p_2 K}{z_1(p_2 - z_1)}$$
$$C_1 = \frac{p_1 - z_2}{R_1 z_2 p_1} \qquad C_2 = \frac{p_2 - z_1}{R_1 p_2 K} \qquad C_3 = \frac{z_1}{R_1 p_2 K} \quad (4)$$

The impedance level is determined by the arbitrary value of r_1. Other controller types (derivative filtered or ideal PID) can be obtained as the limit cases of (4), *i.e.* controller (1) with derivative filtering for $p_2 \to \infty$ ($C_3 = 0$) and ideal PID for both p_1 and $p_2 \to \infty$ ($C_3 = 0$, $R_2 = \infty$, see design example in section 5.2). A permutation of p_1, p_2 and z_1, z_2 (2) allows finding an alternative set of RC values.

Symmetry of controller. The analysis of the transfer function V_{OUT}/V_{REF} results in the following expression:

$$\frac{V_{OUT}}{V_{REF}} = \frac{(R_1+R_4)}{R_1R_4(C_2+C_3)}\frac{(s/z_3+1)(s/z_4+1)(s/z_5+1)}{s(R_2C_1s+1)\left(\frac{C_2C_3}{C_2+C_3}R_3s+1\right)} \quad (5)$$

where we can notice higher numerator order compared to (3). The values of z_3, z_4 are closely related with zeros frequencies z_1, z_2 (3) by complicated cubic equations. The additional zero z_5 causes the high frequency gain tending to unity (see Fig. 5). In other words, controller shown in Fig. 3 has asymmetrical transfer $|V_{OUT}/V_{REF}| \neq |V_{OUT}/V_{FB}|$. This asymmetry is demonstrated by the controller block scheme in Fig. 4 and corresponding bode plot Fig. 5.

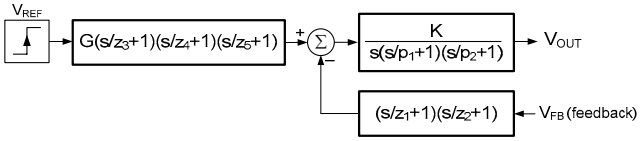

Fig. 4. Block scheme of operational amplifier based controller from Fig. 3.

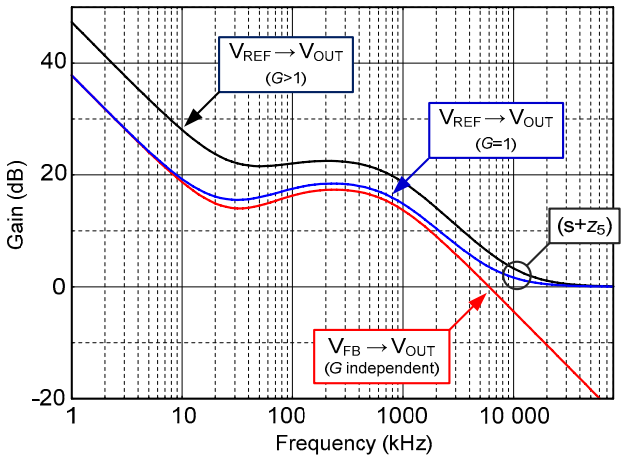

Fig. 5. Comparison of transfers V_{REF}, $V_{FB} \to V_{OUT}$ ($R_1 = 813\,\Omega$, $R_2 = 390\,\Omega$, $R_3 = 2.25\,k\Omega$, $C_1 = 4.51\,nF$, $C_2 = 2.42\,nF$ $C_3 = 100\,pF$, design from [6]).

Controller Bandwidth: equation (3) shows, that resistance R_4 does not influence the closed-loop dynamics. Therefore, the independent gain G can be adjusted without considering the stability of closed-loop system or its quality of disturbances rejections. For instance, while the OpAmp cut-off frequency f_T is not exceeded (see Fig. 2),

the quality of load transient response (disturbance rejection) of DC/DC converter is not affect by the adjusting of the converter steady-state output voltage [6].

4. OTA Based Controller

The controller with operational transconductance amplifier OTA (VCCS) is shown in Fig. 6. It includes one low (–) and one high (+) impedance input (polarities can be reversed). The output is of the high-impedance type and has to be buffered or connected to a high-impedance input.

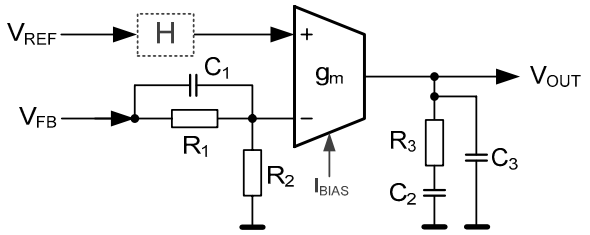

Fig. 6. Controller with operational transconductance amplifier.

The circuit from Fig. 6 allows to realize only the gain $G > 1$. This is caused by the voltage divider $R_1 - R_2$ in the feedback path. The transfer function can be expressed as:

$$\frac{V_{OUT}}{V_{FB}} = \frac{-1}{G}\frac{g_m}{(C_2+C_3)}\frac{(R_1C_1s+1)(R_3C_2s+1)}{s\left(\frac{C_2C_3R_3}{C_2+C_3}s+1\right)\left(\frac{R_1C_1}{G}s+1\right)} \tag{6}$$

where $G=(R_1+R_2)/R_2$ is DC closed-loop (reference) gain (see Fig. 1). In (6), we notice that the second pole is related with nominator zero $1/R_1C_1$ by factor G. This dependency makes impossible the design of controller (form z_1, z_2, p_1, p_2, K) simultaneously with considering the DC gain G. In practice, the reference gain can be slightly adjusted by the value of R_2 (with influence to p_2), or by using an additional block of the gain H (see Fig. 6). Furthermore, the high value of G, together with limited DC-gain of OTA, can affect the closed-loop regulation accuracy (low loop-gain).

The passive components can be computed by means of design equations (c_1, c_2 determine the impedance levels):

$$C_1 = c_1,\ C_2 = c_2 \qquad R_1 = 1/(z_2C_1) \qquad R_2 = 1/\left(C_1(p_1 - z_2)\right)$$
$$R_3 = \frac{1}{z_1C_2} \qquad g_m = \frac{p_1p_2C_2K}{z_2(z_1-p_2)} \qquad C_3 = \frac{z_1C_2}{z_1-p_2} \tag{7}$$

As in previous case, Fig. 6 controller has asymmetrical transfers from V_{FB} and V_{REF} to the output (terms R_1, R_2, C_1, G disappears from (6) in V_{OUT}/V_{REF}). This affects only the low frequency part of characteristic. Optionally, R_1-R_2-C_1 circuit recopied to the (+) input can resolve this problem.

Compared to these inconveniences, controller from Fig. 6 allows simple and independent electrical control of the gain K *via* the transconductance value g_m (trough OTA bias current I_{BIAS}). Beside, as Fig. 6 circuit operates in open-loop, the OTA does not require the frequency compensation, which simplifies the integration in CMOS.

5. CCII based Controller

The main drawback of the circuits of Fig. 3 and Fig. 6 – mismatch of the closed-loop and reference transfers $|V_{OUT}/V_{REF}|$ and $|V_{OUT}/V_{FB}|$ is overcome by the circuit shown in Fig. 6. This presented circuit uses the second generation current conveyor (CCII) containing three terminals: high impedance voltage input **Y,** low impedance voltage output **X**, and high impedance current output **Z**; the terminals transfers are defined as: $v_X = v_Y$, $i_Z = i_X$ and $i_Y = 0$ [9], [10].

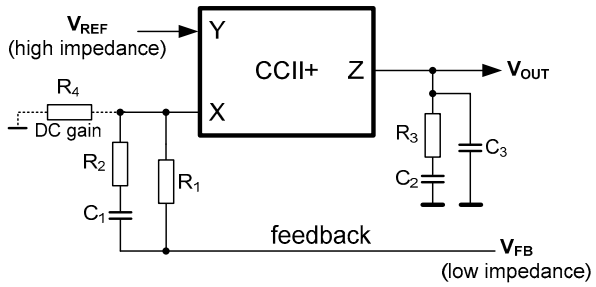

Fig. 7. Second generation current conveyor (CCII) based PID controller.

Similarly to the circuits of Fig. 3 and Fig. 6, the circuit of Fig. 7 contains one low (–) and one high (+) impedance input. The polarities of inputs can be inverted by changing the conveyor type (CCII±). The output (node Z) is a high impedance type and has to be buffered. The controller form (1) can be realized by omitting capacitor C_3.

5.1 Analysis of the Circuit

For the non-inverting conveyor (CCII+), the transfer function V_{OUT}/V_{FB} is identical with transfer function (3) of OpAmp based controller:

$$\frac{V_{OUT}}{V_{FB}} = \frac{-1}{R_1(C_2+C_3)}\frac{(R_3C_2s+1)(C_1(R_1+R_2)s+1)}{s(R_2C_1s+1)\left(\frac{C_2C_3}{C_2+C_3}R_3s+1\right)} \tag{8}$$

As the terminals X and Y are coupled by unity voltage buffer (*i.e.* $V_X = V_Y$), we can simply demonstrate (for $R_4 = \infty$) the symmetry of the circuit. Thus, we can write:

$$\frac{V_{OUT}}{V_{FB}} = -\frac{V_{OUT}}{V_{REF}} \tag{9}$$

In the application requiring independent gain $G > 1$, an optional resistance $R_4 = R_1/(G-1)$ can be added without influencing the closed-loop dynamics (*Eq.* (8) does not contain R_4). For $R_4 < \infty$, the transfer function V_{OUT}/V_{REF} is:

$$\frac{V_{OUT}}{V_{REF}} = \frac{R_1+R_4}{R_1R_4(C_2+C_3)}\frac{(R_3C_2s+1)(C_1(R_1+R_2)s\cdot\gamma+1)}{s(R_2C_1s+1)\left(\frac{C_2C_3}{C_2+C_3}R_3s+1\right)} \tag{10}$$

where γ is nearly unity factor:

$$\gamma = \frac{R_2R_1+R_4R_1+R_4R_2}{(R_1+R_4)(R_1+R_2)} \equiv 1\Big|_{(R_4\to\infty)} \tag{11}$$

Due to the identical transfer functions (3) and (8), the design equations correspond to the OpAmp equations (4).

5.2 Design Considerations, Example

Frequency range: To obtain high bandwidth of the controller (Fig. 2), we require high frequency unity transfer $v_X = v_Y$ of CCII, independent on the X-terminal load impedance. This allows accurate generation of the current I_X, which is then conveyed by simple (wide-frequency range) current mirrors. As the CCII does not require use of the differential input stage (such as OTA or OpAmp), the design of CCII can be based on the alternative structures (see [9 - 12] for instance), allowing to achieve this goal. The fact that the optimization of the output impedance (Z_X) is advantageous compared to the optimization of frequency transfer V_X/V_Y was investigated in [11].

DC gain: In the design of CCII, we also focus on the parasitic resistance R_Z of the terminal Z. The low value of R_Z reduces the DC gain of controller to R_Z/R_1. This, together with the offsets of CCII, affects the steady-state regulation error in the closed-loop.

Design example: The design of Fig. 7 CCII based controller is demonstrated on the controller with filtered derivative (1) presented in [6] (shown also in Fig. 5). The circuit use a CFA (Current-Feedback Amplifier) AD844 [12], composed of one CCII+ and one unity gain voltage buffer connected to the CCII current output node Z. This voltage buffer is used to realize the low-impedance output.

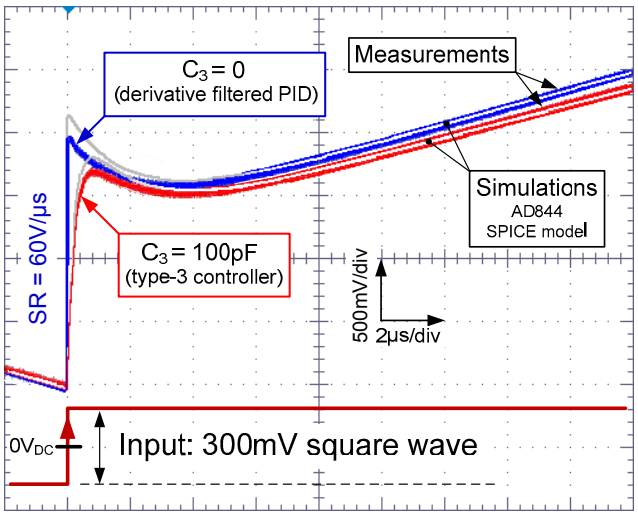

Fig. 8: Measured transient responses of Fig. 7 controller.

The controller presented in [6] has to be arranged in the form of transfer function (2). The zero-pole frequencies are (in rad/s): $z_1 = z_2 = 181 \cdot 10^3$, $p_1 = 568 \cdot 10^3$, $p_2 = \infty$, and gain $K = 4.882 \cdot 10^5$. By employing the equations (4), we determine the limits of terms containing $p_2 \to \infty$: $R_3 = K \cdot R_1/z_1$, $C_2 = 1/(R_1 K)$ and $C_3 = 0$. This allows to compute the component values as: $R_1 = 813\Omega$, $R_2 = 390\Omega$, $R_3 = 2.16\text{k}\Omega$, $C_1 = 4.51\text{nF}$, $C_2 = 2.52\text{nF}$ and $C_3 = 0$.

The measured and simulated transient response is shown in Fig. 8 ($C_3 = 0$). As already mentioned, the controller speed (bandwidth) is inaccurately limited by the active component cut-off frequency. This can influence the resulting dynamic (stability) of the system or its noise immunity (*e.g.* gain at the switching frequency of DC/DC converter). In [6], supplementary pole $p_2 = 4.638 \cdot 10^6$ rad/s realized by capacitor C_3 was added for more accurate control of high frequency gain (type-3 regulation). For such controller, the values can be computed directly from equations (4) and corresponds to the values mentioned in caption Fig. 5. Measured characteristic is shown in Fig. 8.

Conclusion

We presented the detailed overview of circuits realizing PID controllers with single OpAmp, OTA and CCII. The analysis of first two structures pointed to the asymmetrical transfer functions form V_{REF} and V_{FB} inputs to the output V_{OUT}. This inconvenience is overcome by presented circuit based on the CCII, whose utilization allows to employ alternative current-mode structures in the CMOS integration. The target application concerns the switched DC/DC converters intended for the new mobile phone power management platform in 40nm CMOS.

Acknowledgements

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