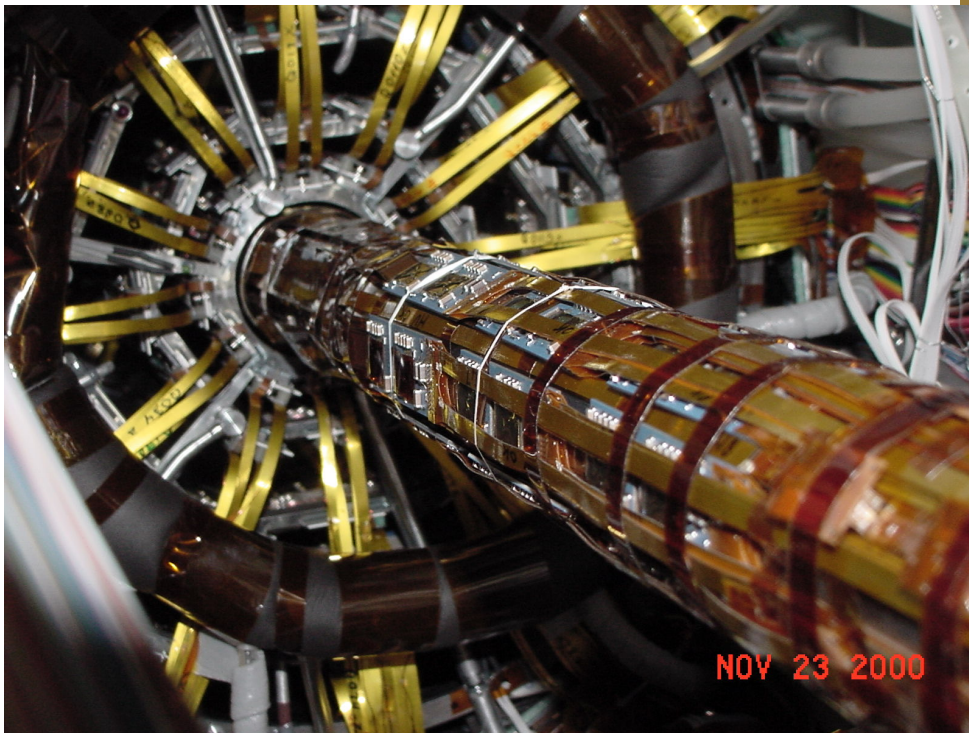
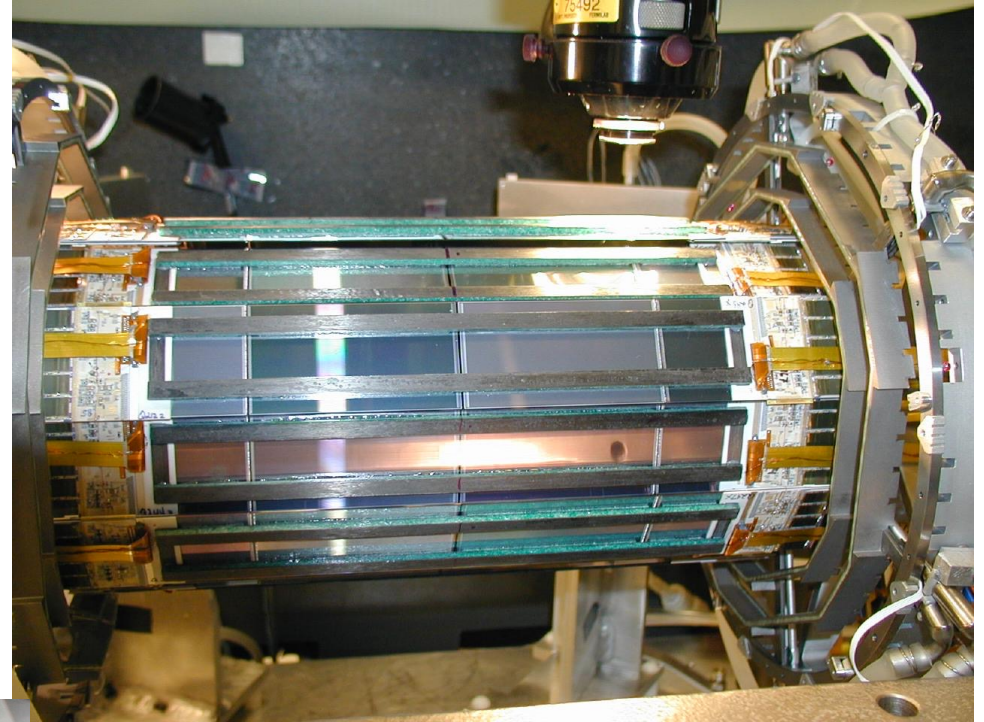


# Silicon Particle Detectors

– Why they are useful  
and How they work.



William Trischuk  
University of Toronto/CDF  
May 20, 2004

Many Thanks to Rainer Wallny (UCLA)  
Alan Honma, CERN and  
Steve Worm, Rutgers  
Gino Bolla, Purdue  
Christian Joram, CERN

# Outline

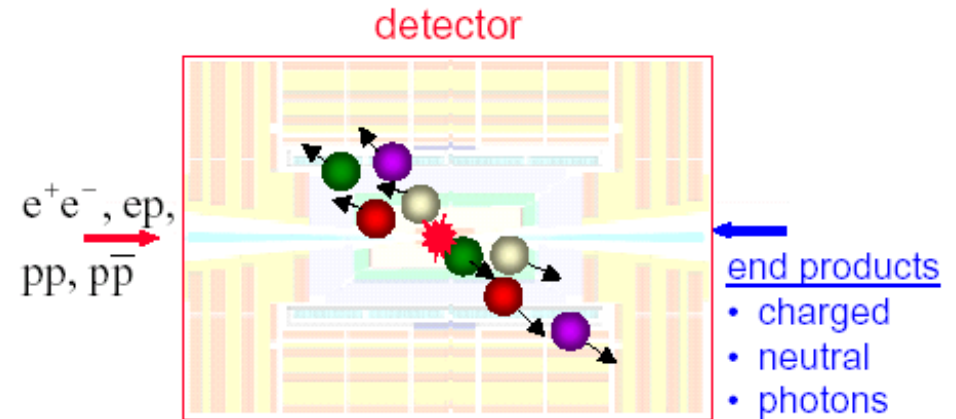
- o Introduction
  - Overview of HEP Detectors
- o Why Silicon ?
- o Semiconductor Basics
  - Band-gap, PN junction
  - Silicon strip detectors
  - Signal formation in a silicon sensor
- o Some Technicalities
  - Wafer Production
  - Wire Bonding
- o Conclusions

## The Intro .....

# Particle Detection

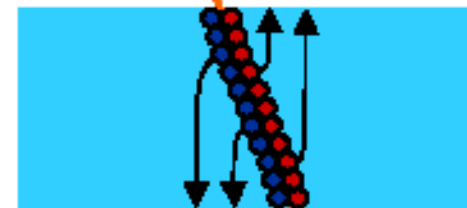
The 'ideal' detector should provide ....

- o Coverage of **full solid angle**
- o Measurement of **momentum** and **energy** (E,p)
- o Detect, **track** and **identify** all particles (**mass, charge**)
- o Fast response, **no deadtime**



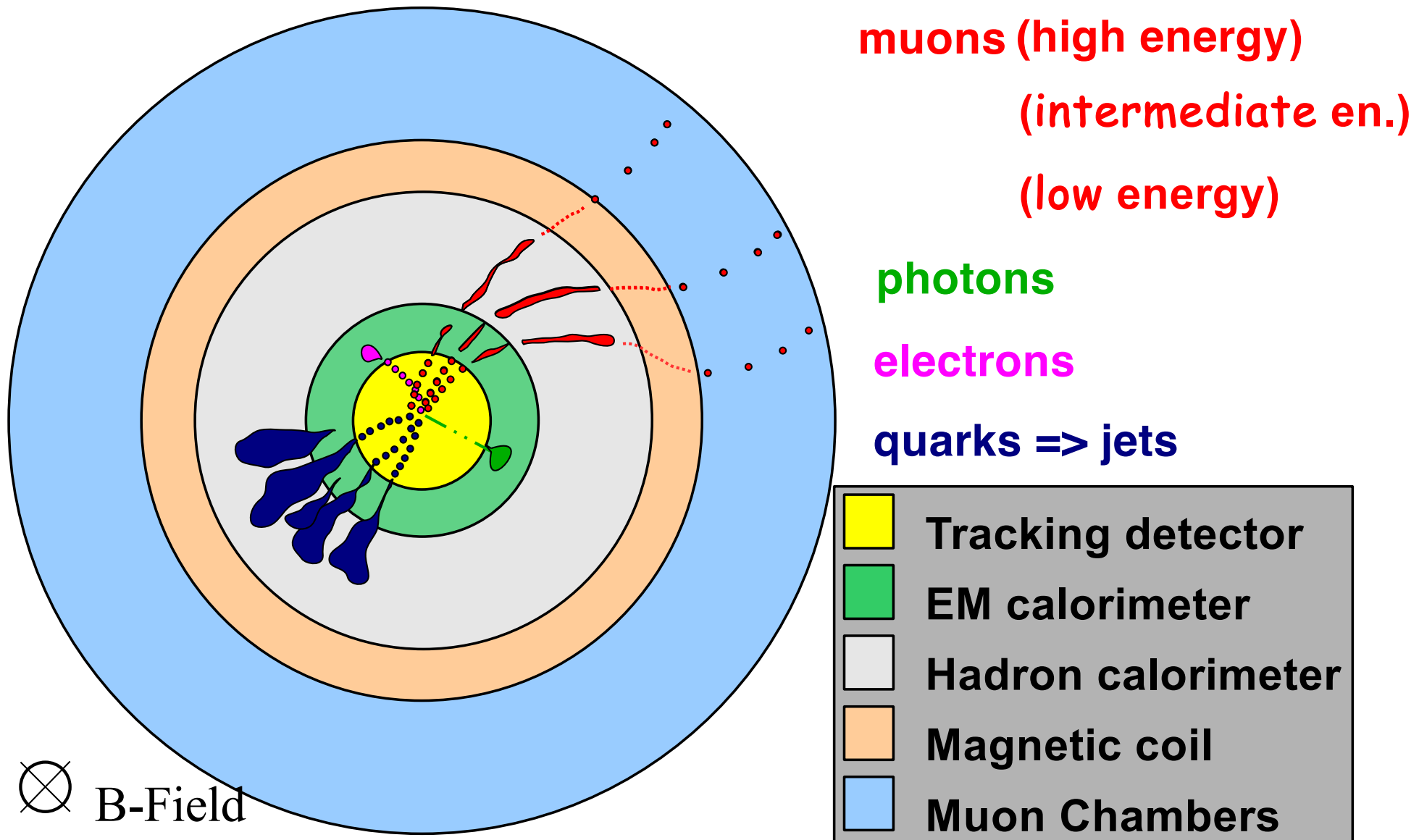
## Particles are detected through interactions with matter

- o Many different physical principles are involved
- o For charged particles predominantly excitation and ionization of detector medium



**Tracker (p): Thin (low-Z) material (gas, liquid, solid (Si) )**  
**Calorimeter (E): High-Z material (absorber)**

# Operating Principles of Particle Physics Detectors at Colliders



# Tracking Chambers with Solid Media

- o Ionization chamber medium could be gas, liquid, or solid
  - Some technologies (ie. bubble chambers) not applicable in collider environments

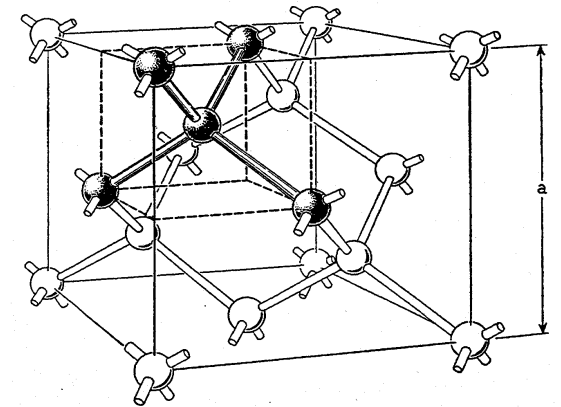
	Gas	Liquid	Solid
Density	Low	Moderate	High
Atomic number	Low	Moderate	Moderate
Ionization Energy	Moderate	Moderate	Low
Signal Speed	Moderate	Moderate	Fast

- o High-precision tracking advantages with solid media
  - Easily ionized, relatively large amount of charge
  - Locally high density means less charge spreading
  - Fast readout possible

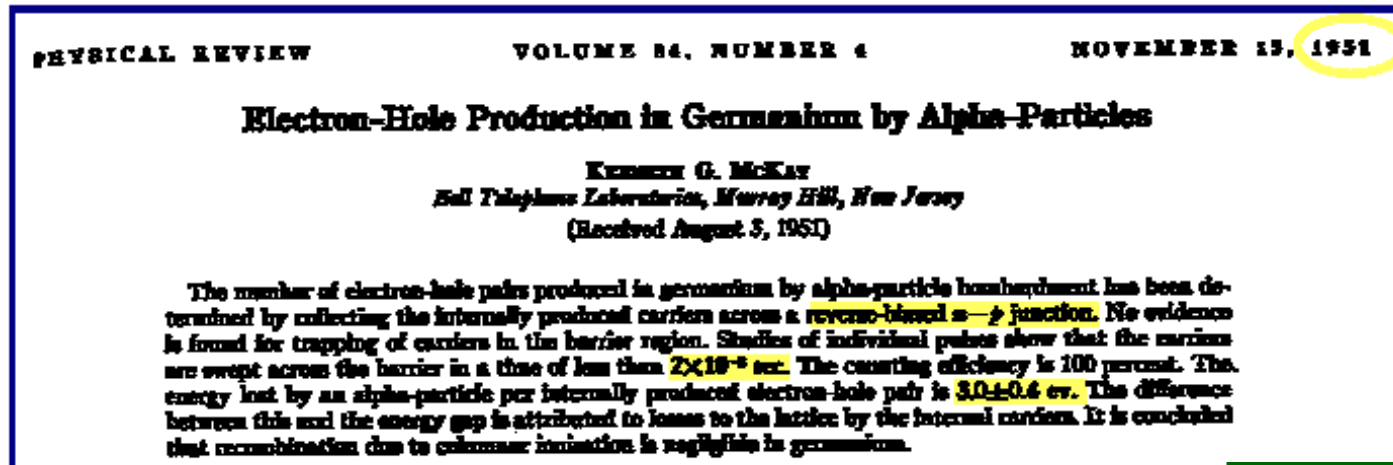
“Solid-state detectors require high-technology devices built by specialists and appear as black boxes with unchangeable characteristics.” -Tom Ferbel (detector expert) 1987

# Why Silicon?

- **Electrical properties are good**
  - Forms a native oxide with excellent electrical properties
  - Ionization energy is small enough for easy ionization, yet large enough to maintain a low dark current
- **Mechanical properties are good**
  - Easily patterned and read out at small dimensions
  - Can be operated in air and at room temperature
  - Can assemble into complex geometries
- **Availability and experience**
  - Significant industrial experience and commercial applications
  - Readily available at your nearest beach

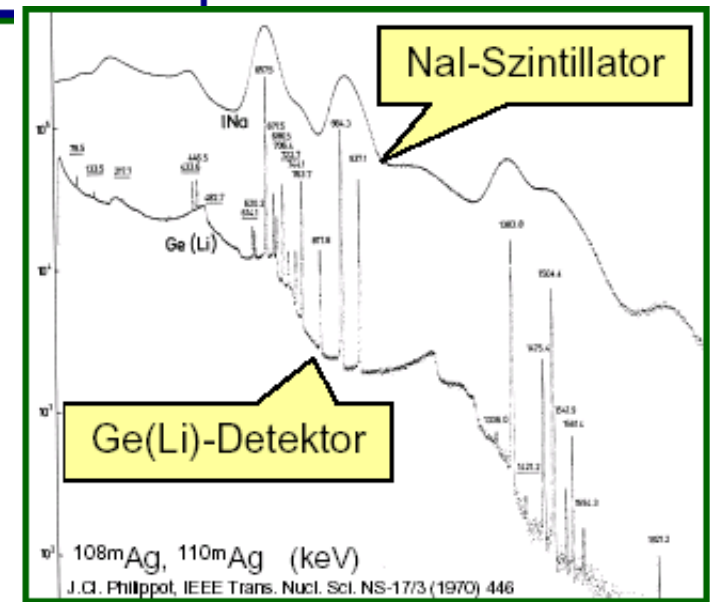


# The Idea is Not Quite New ...



Semiconductors used since 1950s for energy measurement in nuclear physics

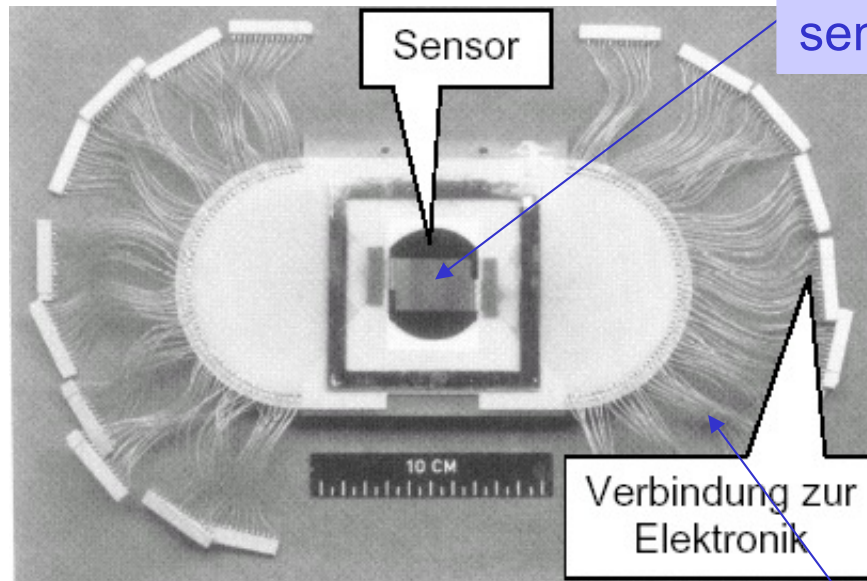
- o Precision position measurements up until 1970s done with emulsions or bubble chambers
  - > limited rates, no triggering
- o Traditional gas detectors: limited to 50-100  $\mu\text{m}$
- o First silicon usage for precision position measurement: NA11 at CERN, 1980





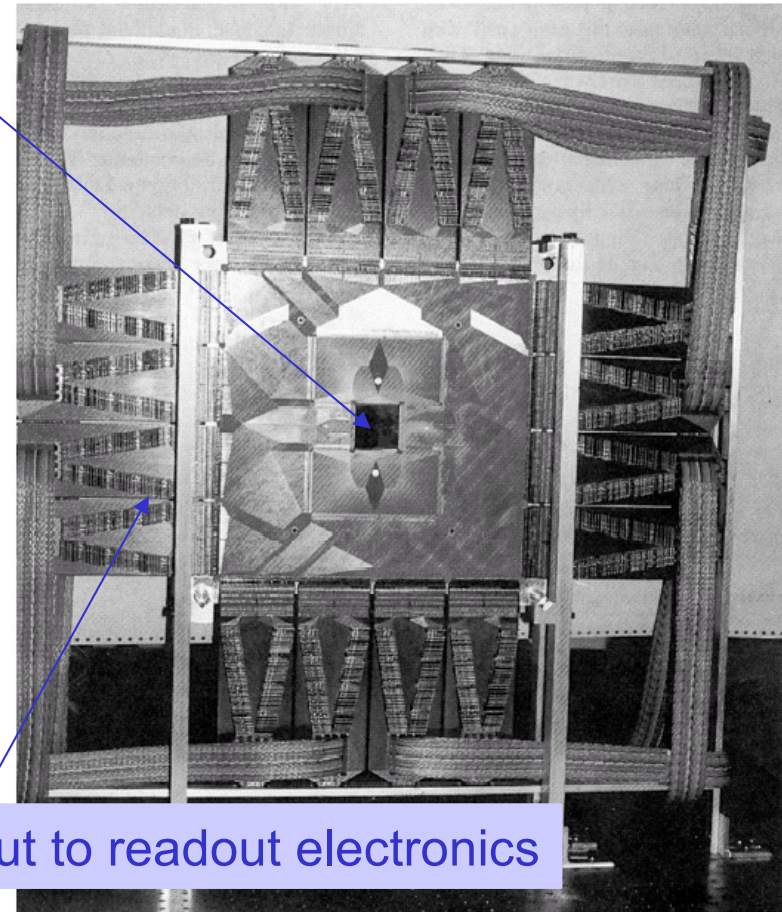
# Pioneering Silicon Strip Detectors

NA11 (CERN 1981)



- o 24x36 mm<sup>2</sup> active area
- o 8 layers of silicon
- o 1m<sup>2</sup> readout electronics!

E706 (FNAL 1987)

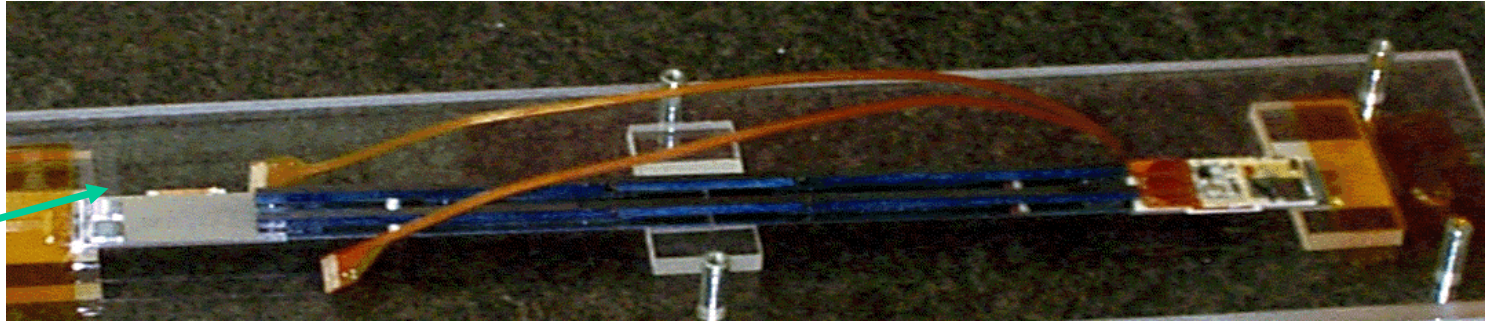


- o 50x50 mm<sup>2</sup> active area

Silicon sensor and readout electronics technology closely coupled

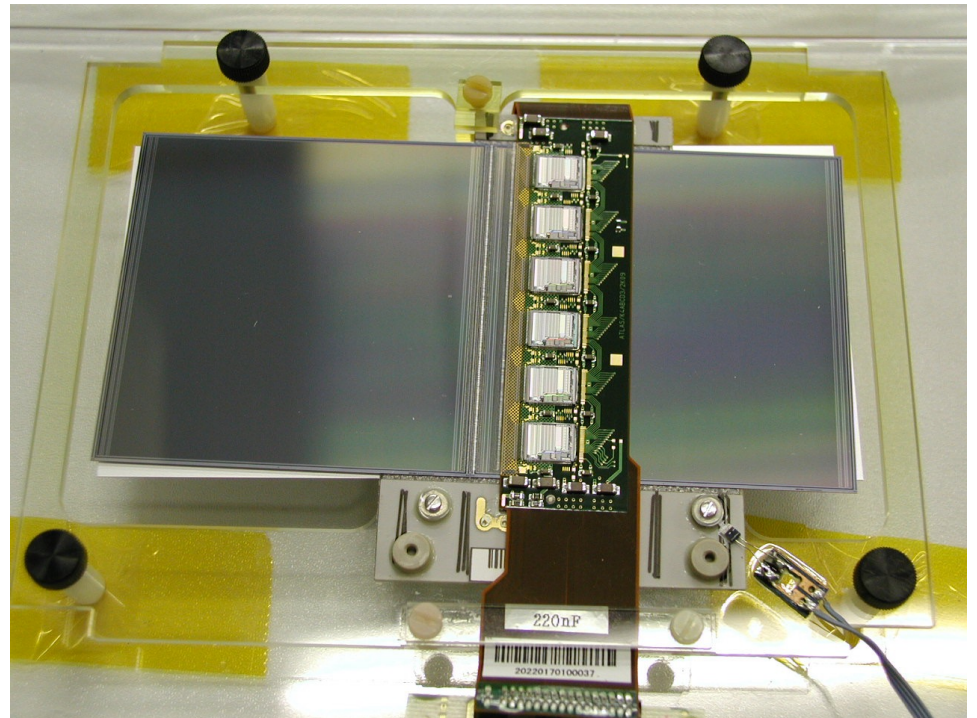
⇒ with electronics miniaturization (transistors, ICs, ASICs ...) silicon quickly took off ...

# Contemporary Silicon Detector Modules



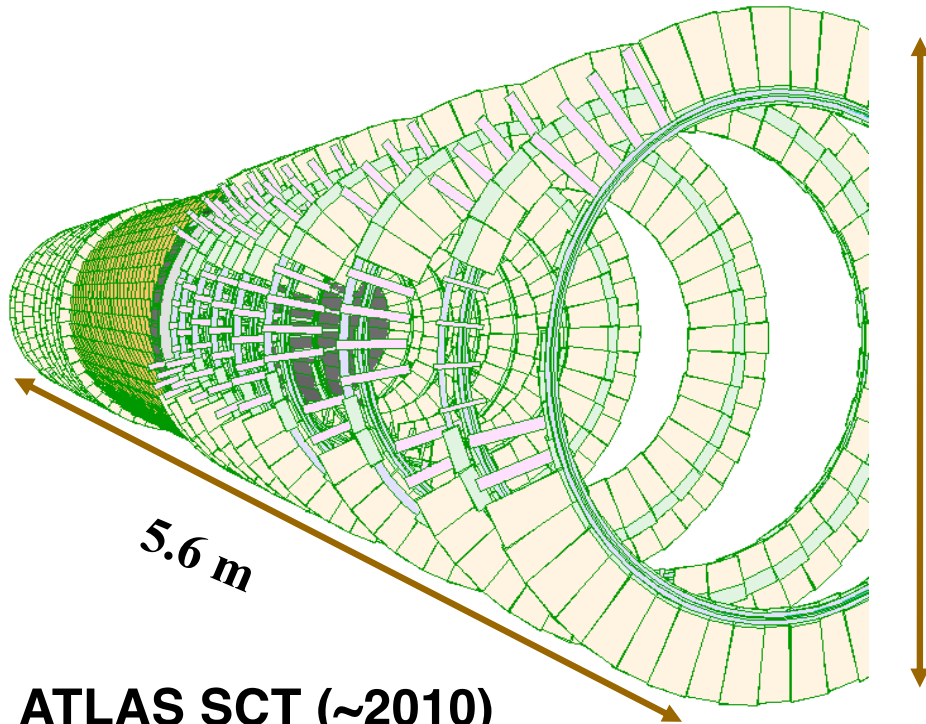
CDF SVX IIa half-ladder: two silicon sensors with readout electronics (SVX3b analog readout chip) mounted on first sensor

ATLAS SCT barrel module: four silicon sensors with center-tapped readout electronics (ABCD binary readout chip)



Silicon sensor and readout chip development intimately related  
BUT will concentrate on silicon only here ...

# Large 'Contemporary' Silicon Systems



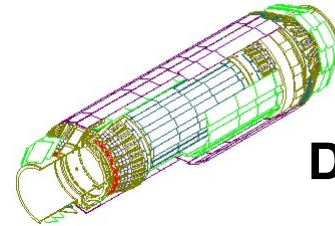
## ATLAS SCT (~2010)

4088 modules

~ 61 m<sup>2</sup> silicon area

15,392 silicon wafers

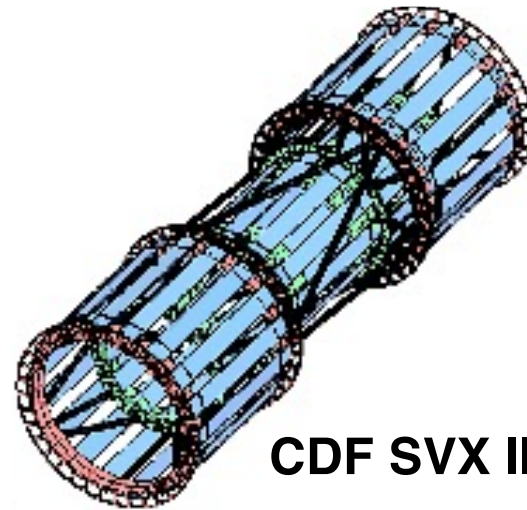
~ 6.3M readout channels



## DELPHI (1996)

~ 1.8m<sup>2</sup> silicon area

175 000 readout channels



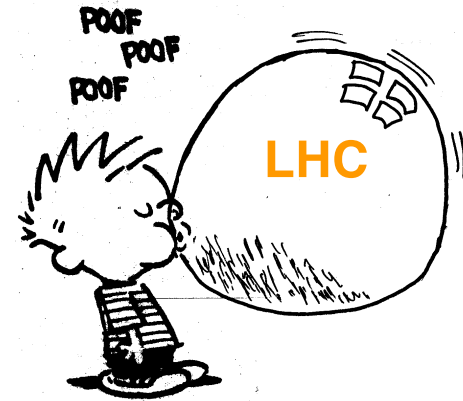
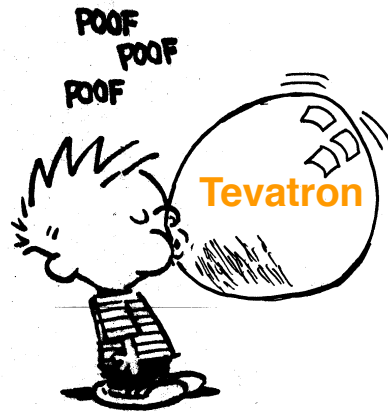
## CDF SVX IIa (2001-)

~ 11m<sup>2</sup> silicon area

~ 750 000 readout channels



# Large Silicon Detector Systems ...



Whoops...

P.Collins, ICHEP 2002

Now building ATLAS/CMS replacement trackers  
5x as many readout channels – roughly same area as originals

# The Basics .....

20/5/2004

William Trischuk,

# Semiconductor Basics - Band Gap

- In a gas, electron energy levels are discrete. In a solid, energy levels split and form a nearly-continuous band.

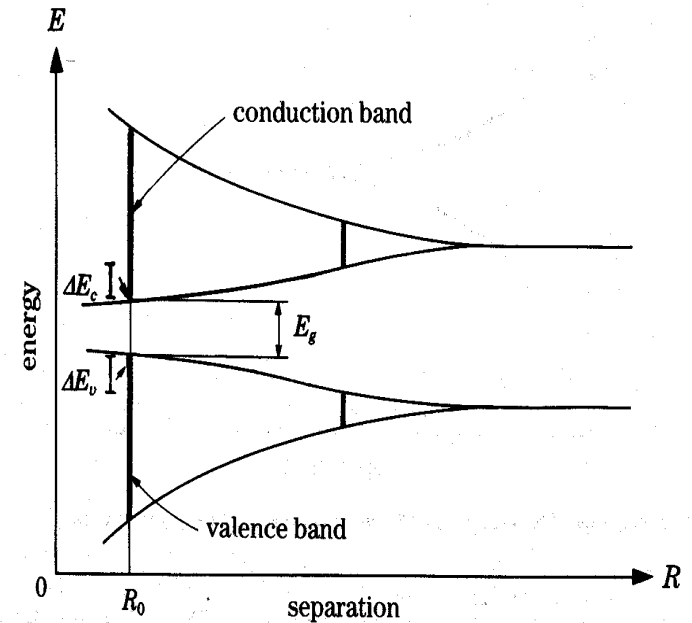
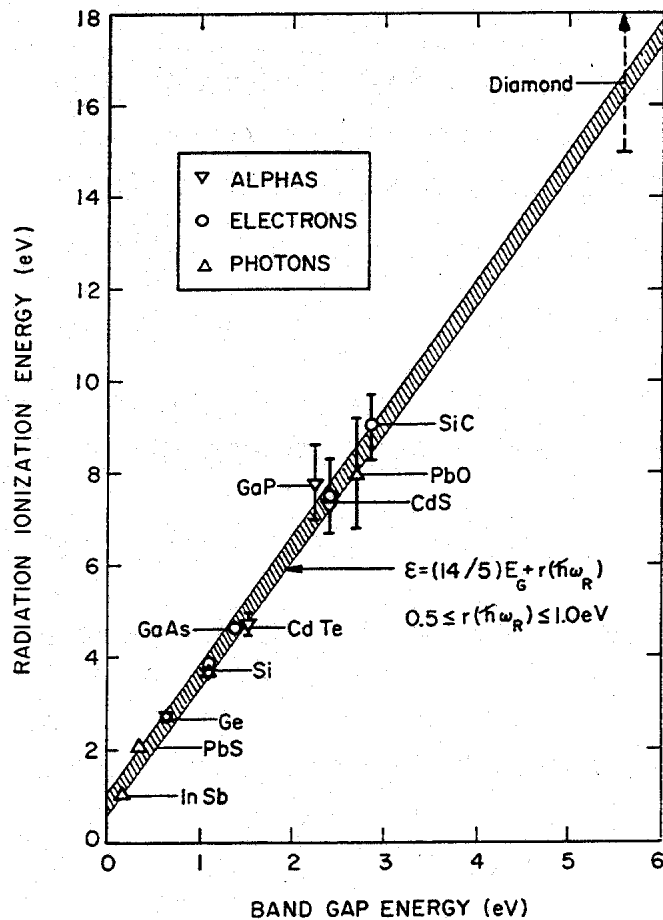


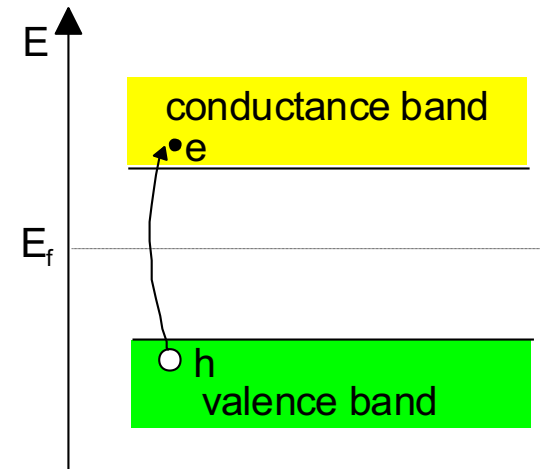
Fig. 1.2. Energy levels in a system of  $N$  atoms as a function of the separation  $R$  between the atoms. The equilibrium atomic separation is  $R_0$ .

- If the gap is large, the solid is an insulator. If there is no gap, it is a conductor. A semiconductor results when the gap is small.
- For silicon, the band gap is 1.1 eV, but it takes 3.6 eV to ionize an atom. The rest of the energy goes to phonon excitations (heat).

William Trischuk,

# Semiconductor Basics - Principle of Operation

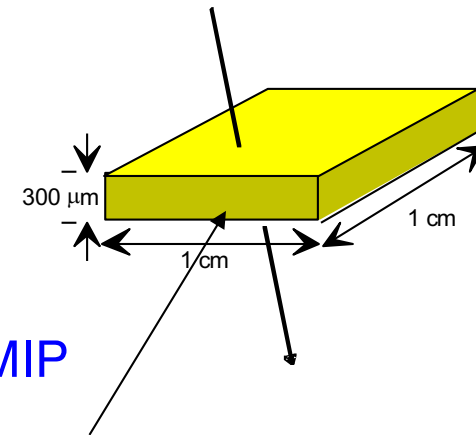
- Basic motivation: charged particle position measurement
- Use ionization signal ( $dE/dx$ ) left behind by charged particle passage



- In a semiconductor, ionization produces electron-hole pairs
- Electric fields drift electrons and holes to oppositely electrodes

BUT:

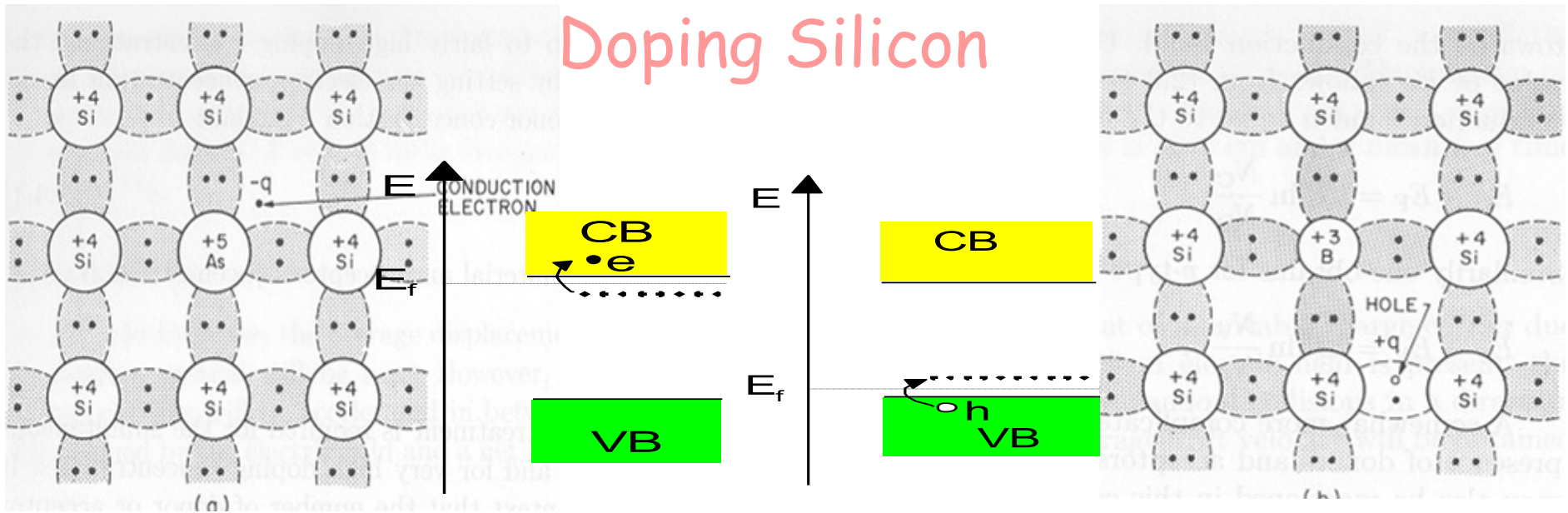
- In pure intrinsic (undoped) silicon, many more free charge carriers than those produced by a charged particle.
  - Have  $4.5 \times 10^8$  free charge carriers; only  $3.2 \times 10^4$  produced by MIP
- Electron-hole pairs quickly re-combine ...



**Need to deplete free charge carriers and separate e-holes 'quickly' !**



# Doping Silicon



## n-type:

- In an n-type semiconductor, negative charge carriers (electrons) are obtained by adding impurities of donor ions (eg. Phosphorus (type V))
- Donors introduce energy levels close to conduction band thus almost fully ionized  $\Rightarrow$  Fermi Level near CB

Electrons are the majority carriers.

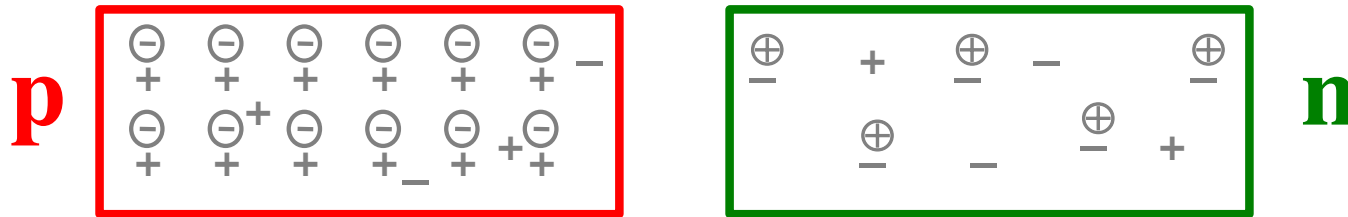
## p-type:

- In a p-type semiconductor, positive charge carriers (holes) are obtained by adding impurities of acceptor ions (eg. Boron (type III))
- Acceptors introduce energy levels close to valence band thus 'absorb' electrons from VB, creating holes  $\Rightarrow$  Fermi Level near VB.

Holes are the majority carriers.

# Semiconductor Basics - pn Junction

Exploit the properties of a **p-n junction** (diode) to collect ionization charges

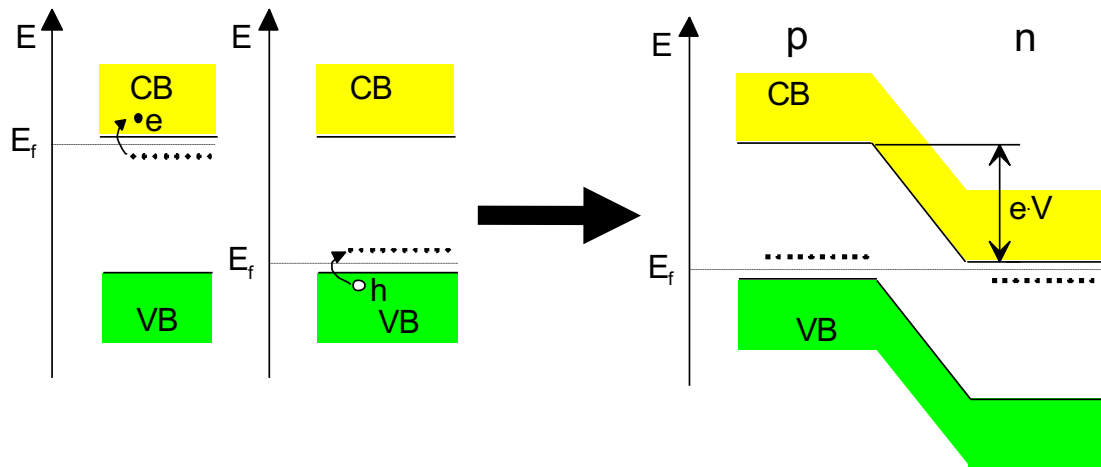


When brought together to form a junction, a gradient of electron and hole densities results in a diffuse migration of majority carriers across the junction. Migration leaves a region of net charge of opposite sign on each side, called the depletion region (depleted of charge carriers).

Electric field set up prevents further migration of carriers resulting in potential difference  $V_{bi}$

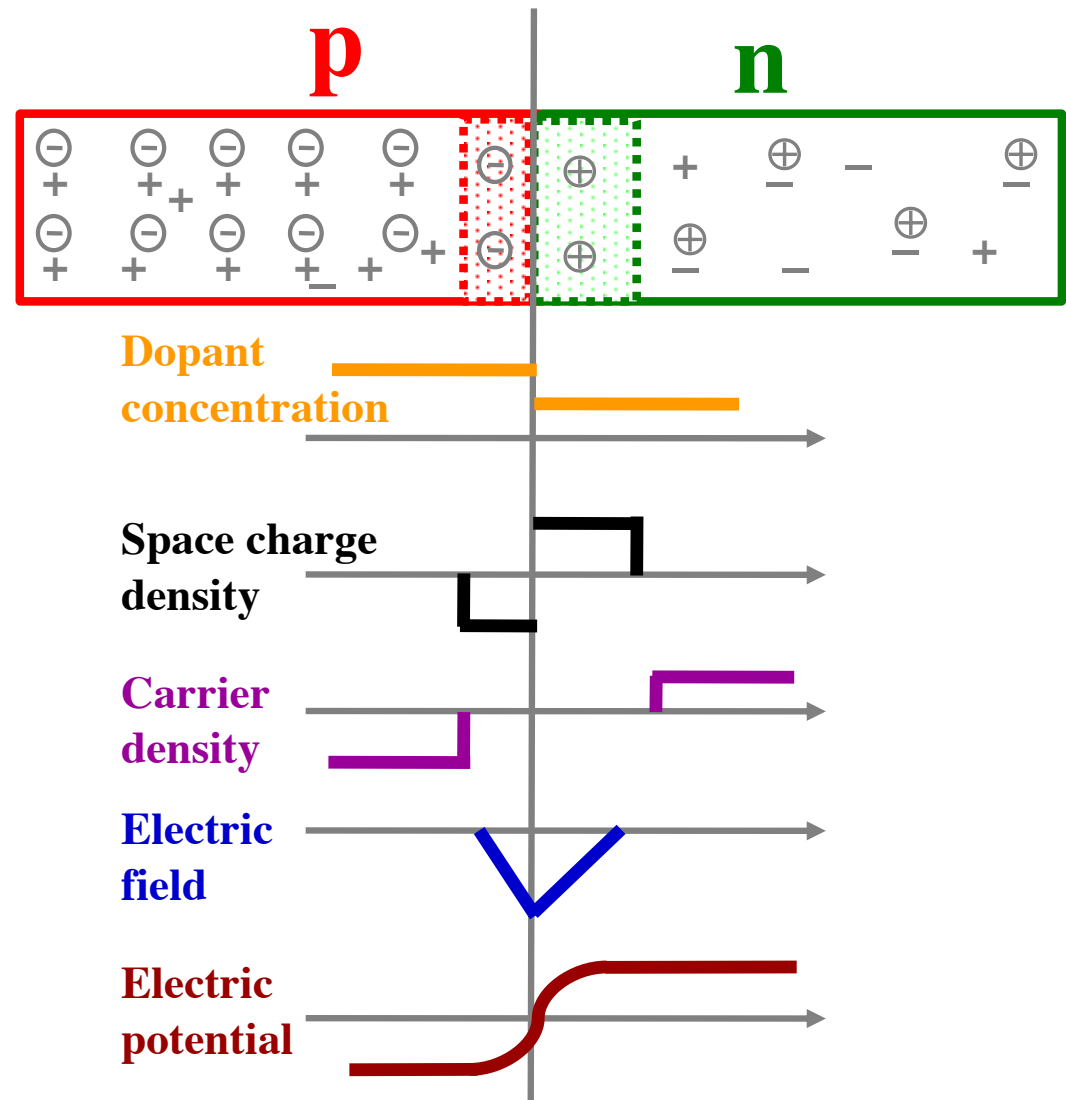
Another way to look at it:

Fermi-Levels need to be adjusted so thus energy bands get distorted => potential  $V_{bi}$



# pn-Junction Overview

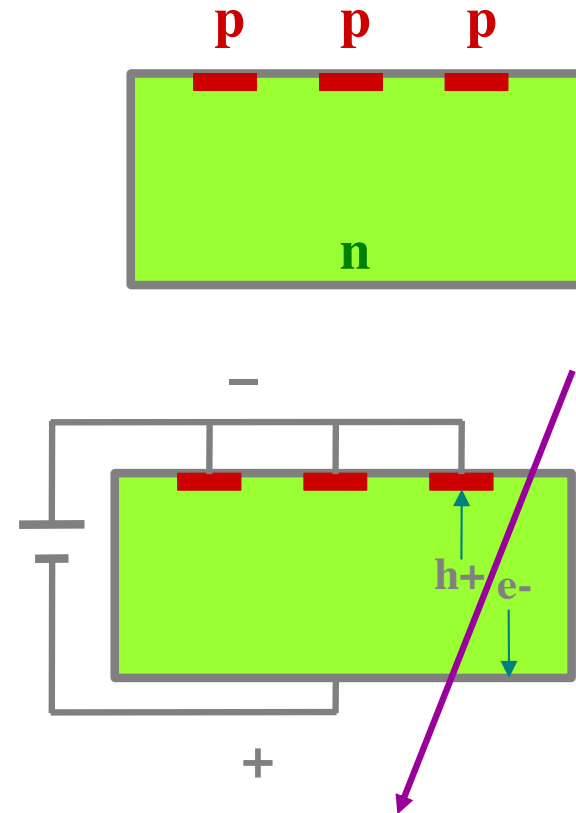
- o p-type and n-type doped silicon forms a region that is depleted of free charge carriers
- o The depleted region contains a non-zero fixed charge and an electric field. In the depletion zone, electron – hole pairs won't recombine but rather drift along field lines
- o Artificially increasing this depleted region by applying a **reversed bias voltage** allow charge collection from a larger volume



William Trischuk,

# How to Build a Strip Detector

If we make the p-n junction at the surface of a silicon wafer with the bulk being n-type (you could also do it the opposite way), we then need to extend the depletion region throughout the n bulk to get maximum charge collection by applying a reverse bias voltage.



# Properties of the Depletion Zone

- Depletion width is a function of the bulk resistivity, charge carrier mobility and the magnitude of reverse bias voltage  $V_b$ :

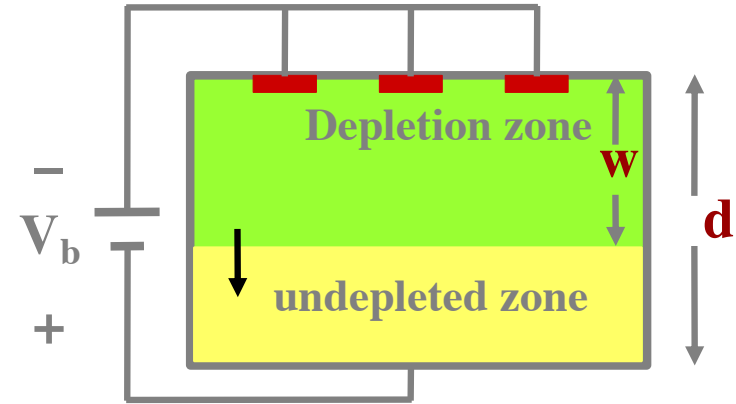
$$w = \sqrt{2 \epsilon \rho \mu V_b}$$

where  $\rho = 1 / q \mu N$  for doped material where  $N$  is the doping concentration and  $q$  is the charge of the electron

- The bias voltage needed to completely deplete a device of thickness  $d$  is called the **depletion voltage**,  $V_d$

$$V_d = d^2 / (2 \epsilon \rho \mu)$$

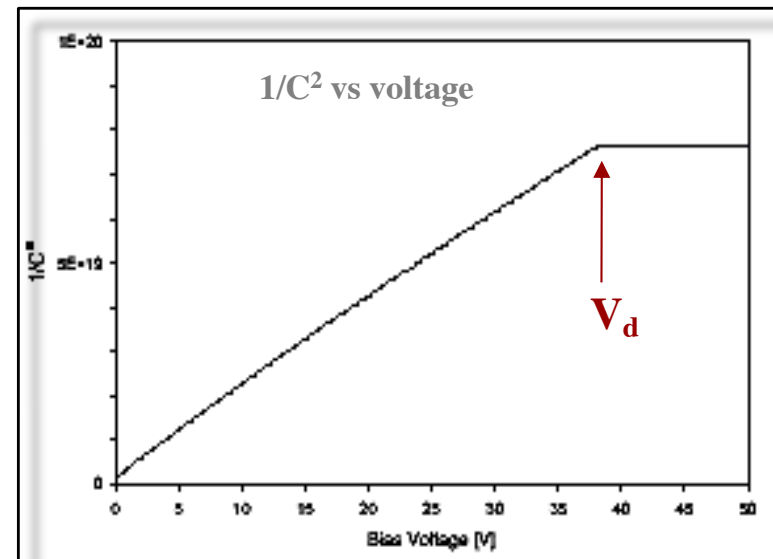
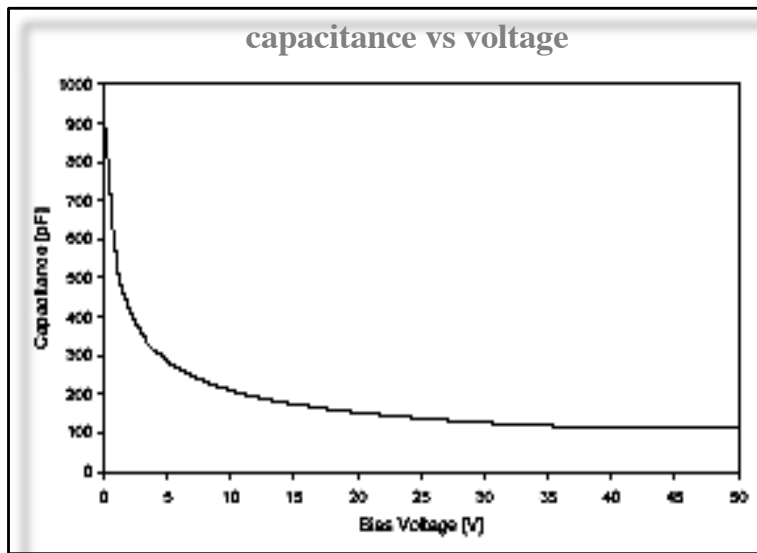
- Need a higher voltage to fully deplete a low resistivity material.
- A higher voltage is needed for a p-type bulk since the carrier mobility of holes is lower than for electrons (450 vs 1350 cm<sup>2</sup>/ V·s)



# Properties of the Depletion Zone (cont'd)

- One normally measures the depletion behaviour (finds the depletion voltage) by measuring the capacitance versus reverse bias voltage. The capacitance is simply the parallel plate capacity of the depletion zone.

$$C = A \sqrt{\epsilon / 2\rho\mu V_b}$$



# Leakage Current

Two main sources of (unwanted) current flow in reversed-biased diode:

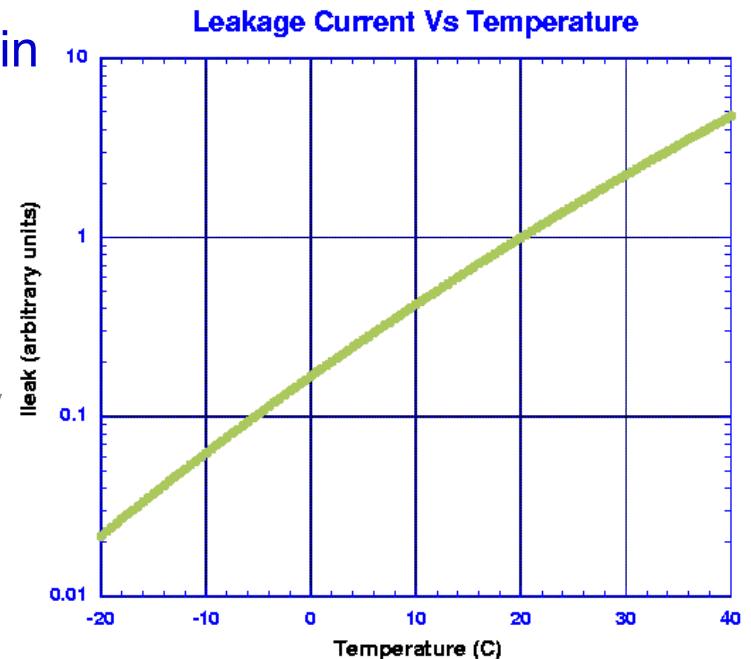
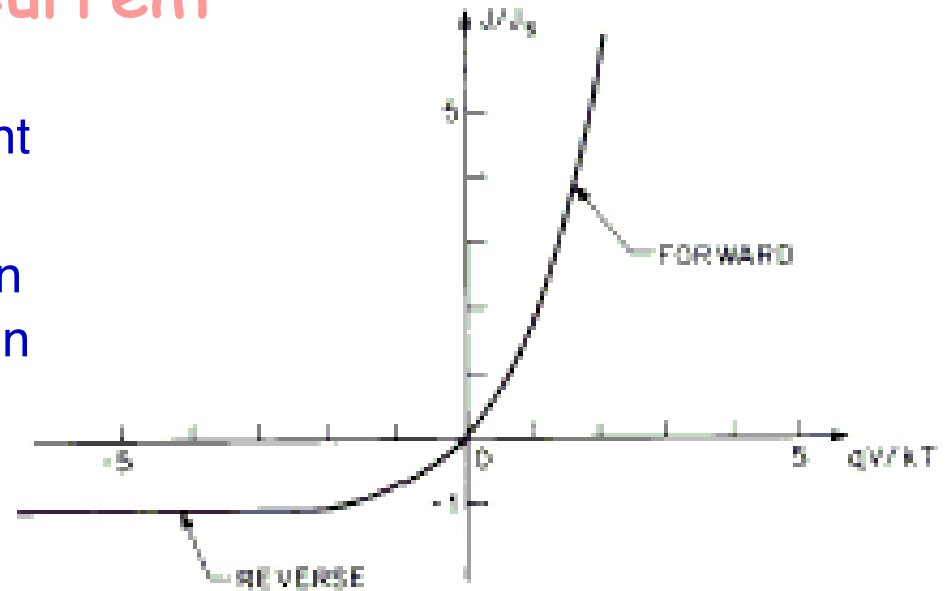
- Diffusion current, charge generated in undepleted zone adjacent to depletion zone diffuses into depletion zone (otherwise would quickly recombine)

negligible in a fully depleted device

- Generation current  $J_g$ , charge generated in depletion zone by defects/contaminants

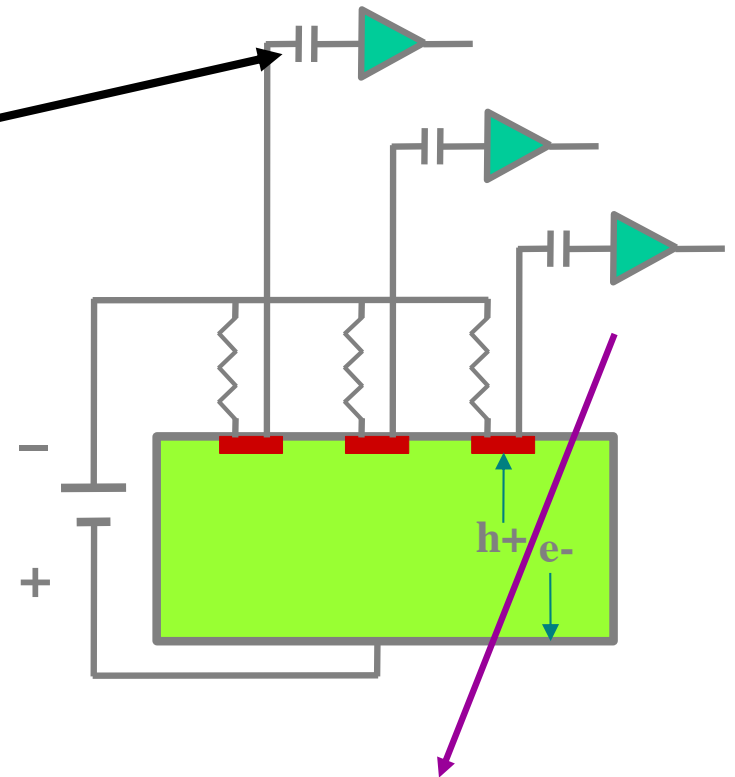
$$J_g \propto \exp(-b/kT)$$

Exponential dependence on temperature due to thermal dependence of e-h pair creation by defects in bulk. Rate is determined by nature and concentration of defects.



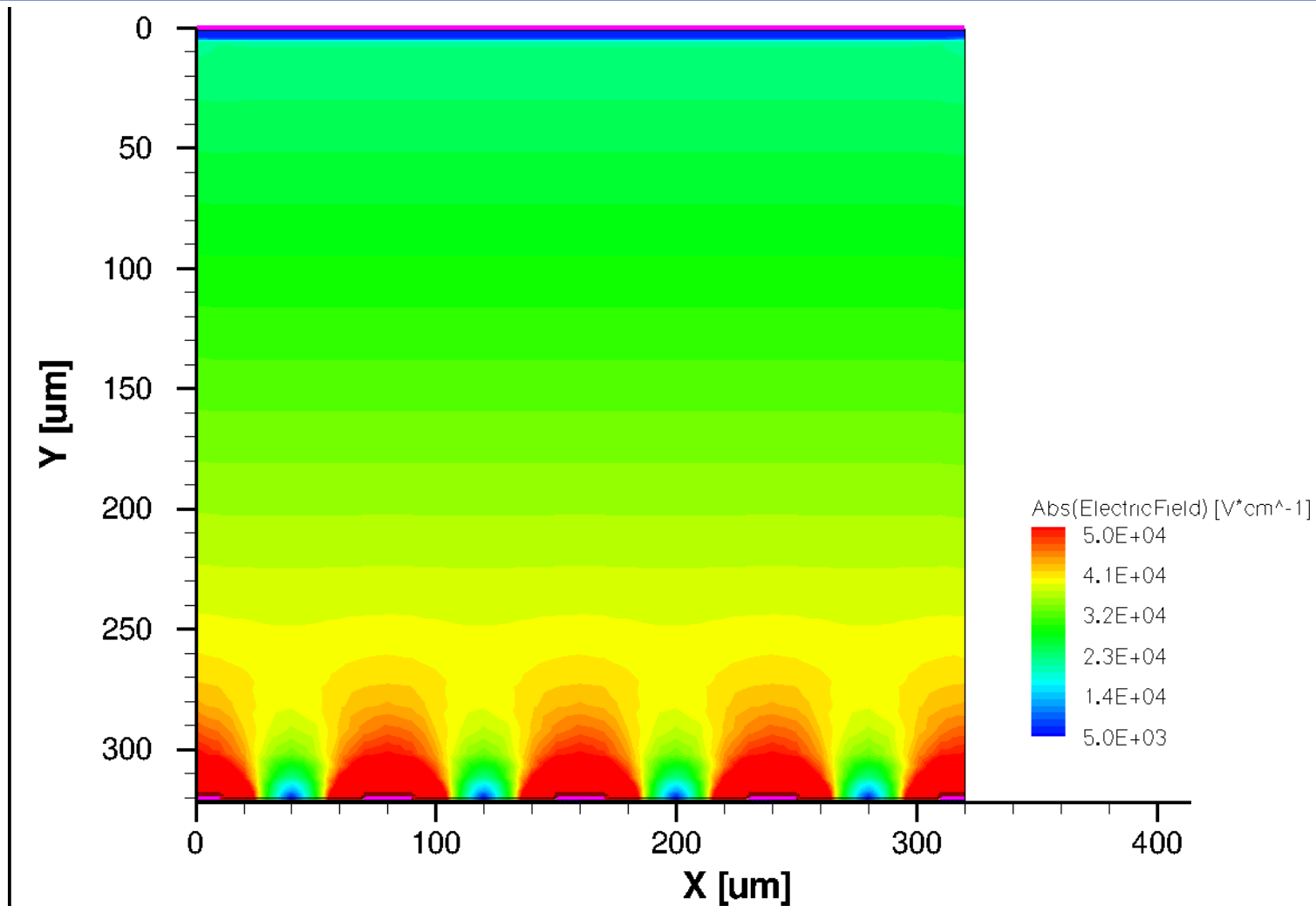
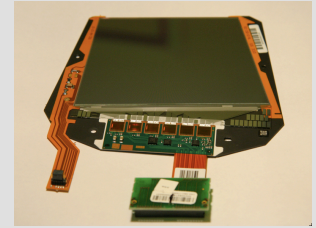
# Bias Resistor and AC Coupling

- Need to isolate strips from each other and collect/measure charge on each strip  $\square$  high impedance bias connection (resistor or equivalent)
- Usually want to AC (capacitively) couple input amplifier to avoid large DC input from leakage current.
- Both of these structures are often integrated directly on the silicon sensor. Bias resistors via deposition of doped polycrystalline silicon, and capacitors via metal readout lines over the implants but separated by an insulating dielectric layer ( $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ).

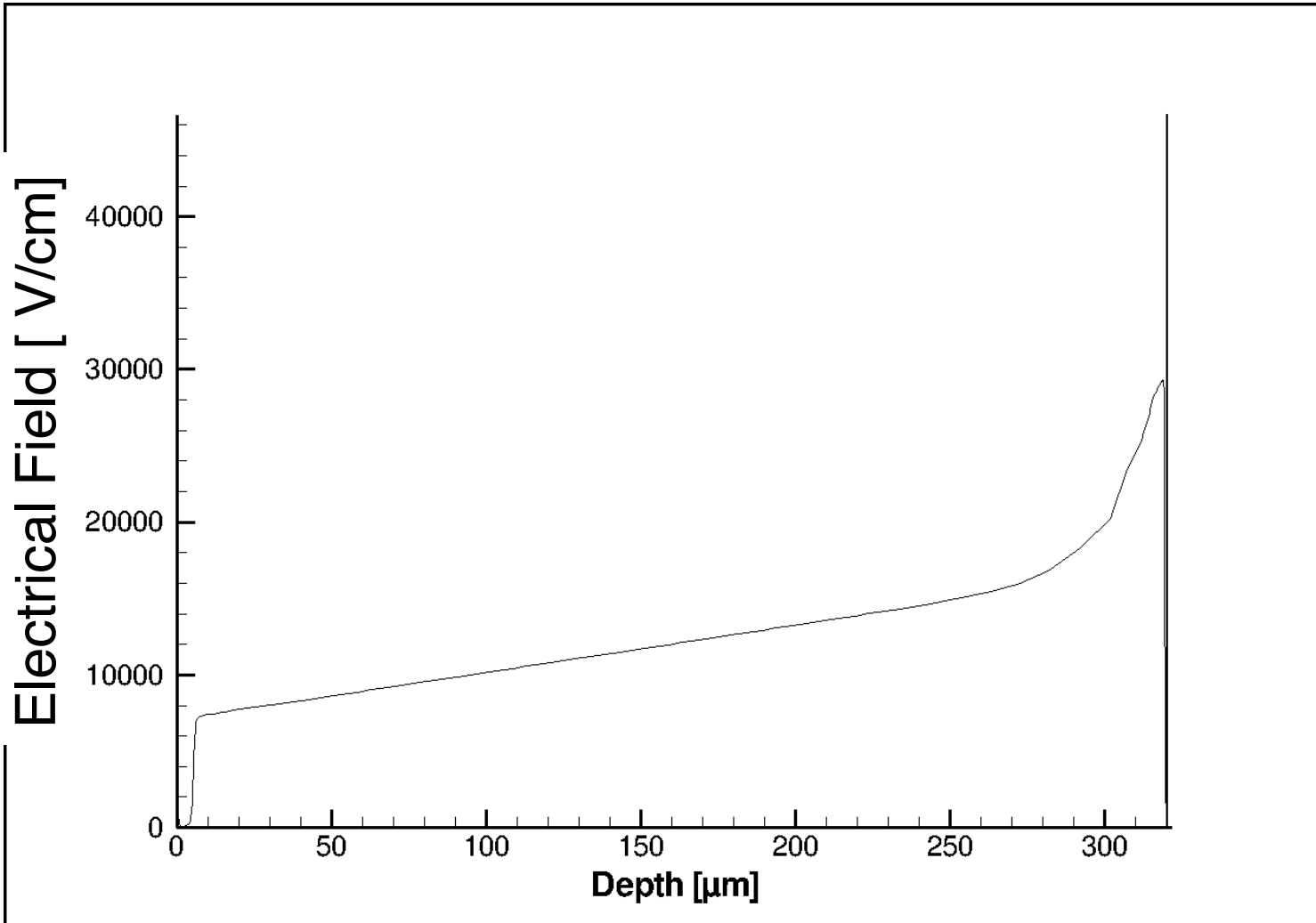




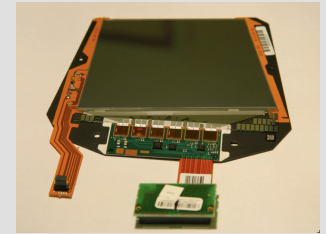
## 2.2 Electrical Field Configuration of a Strip Sensor



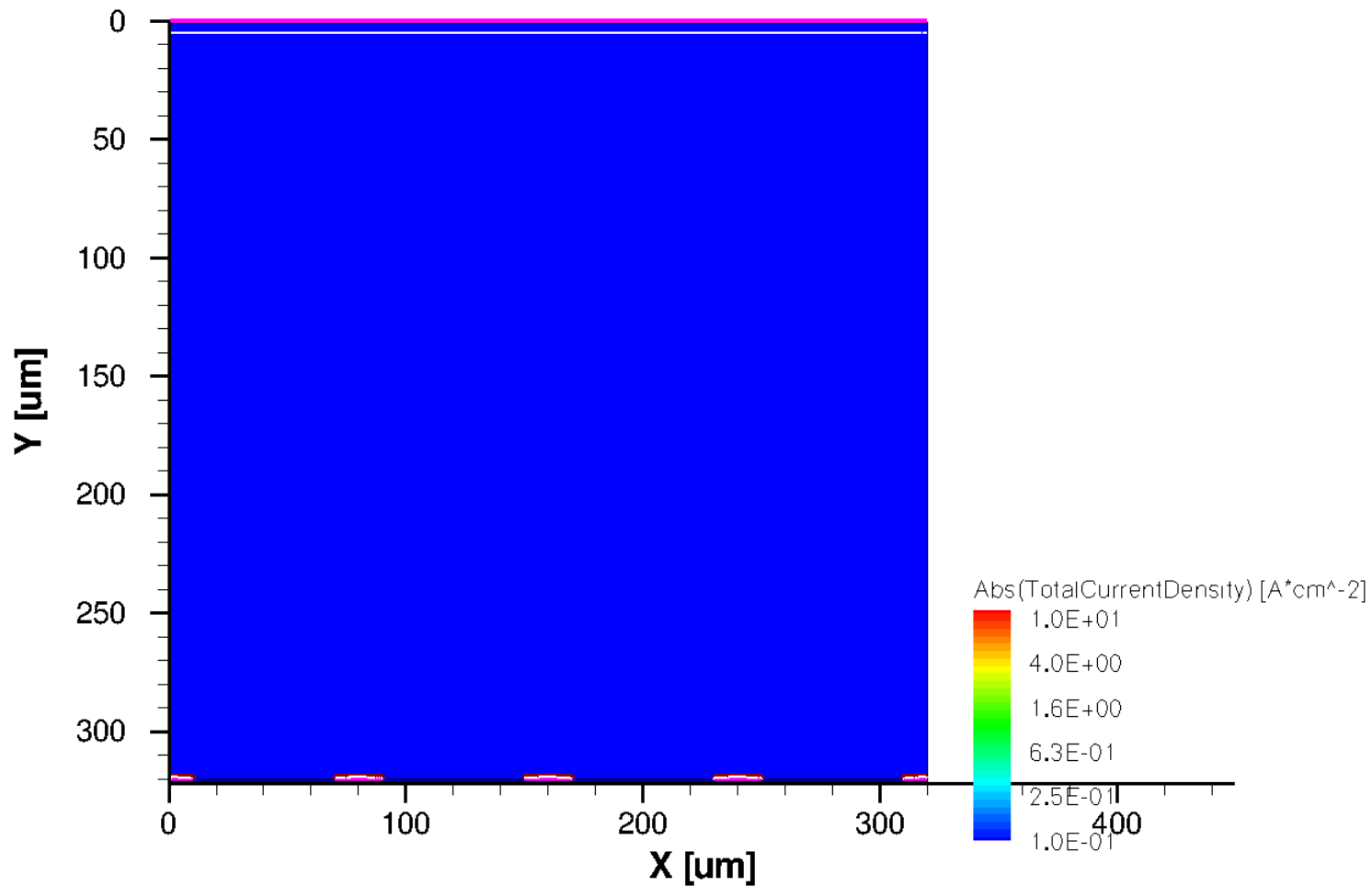
## 2.2. Electrical Field across a Strip



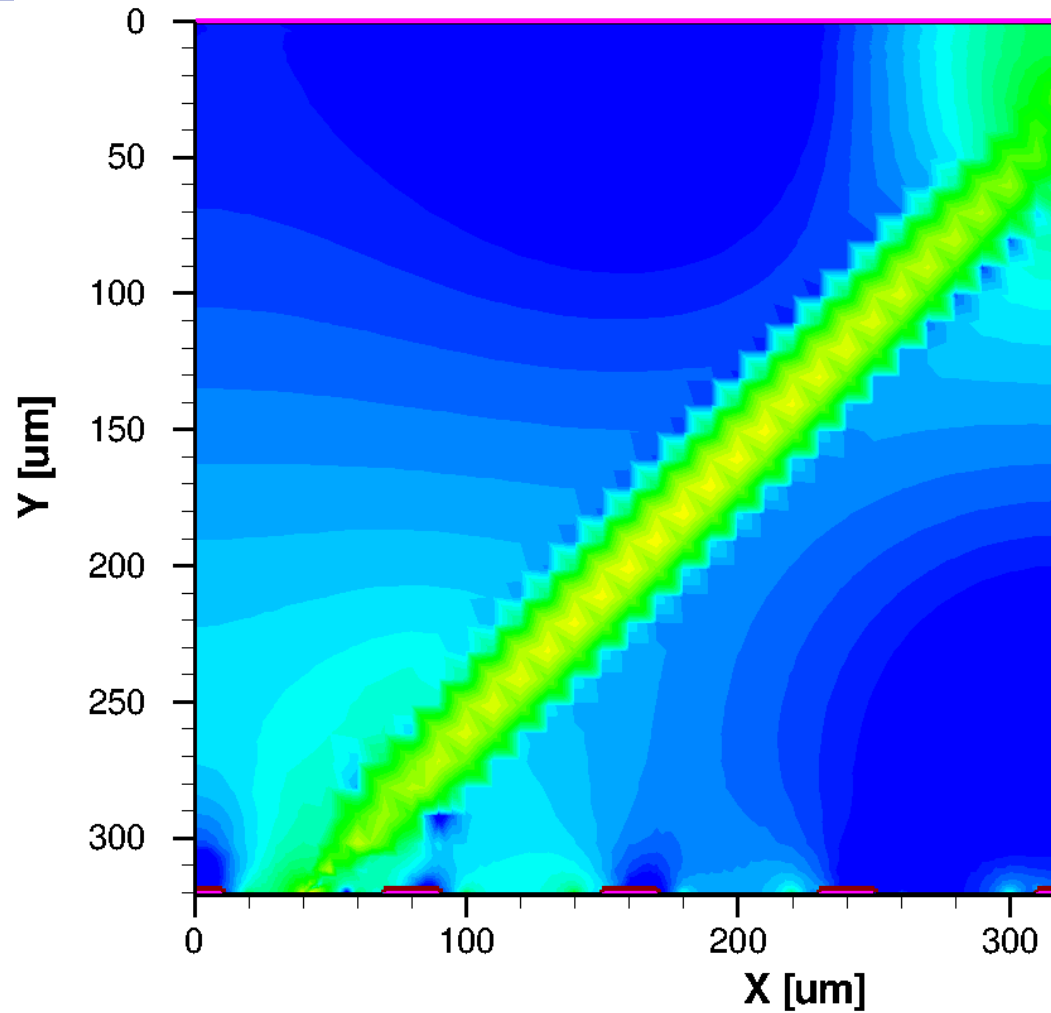
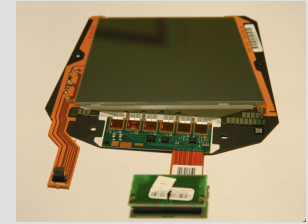
## 2.2. Simulated Current Density Ionizing particle with 45° angle t=0 s



Simulation Thomas.Eichhorn@kit.edu

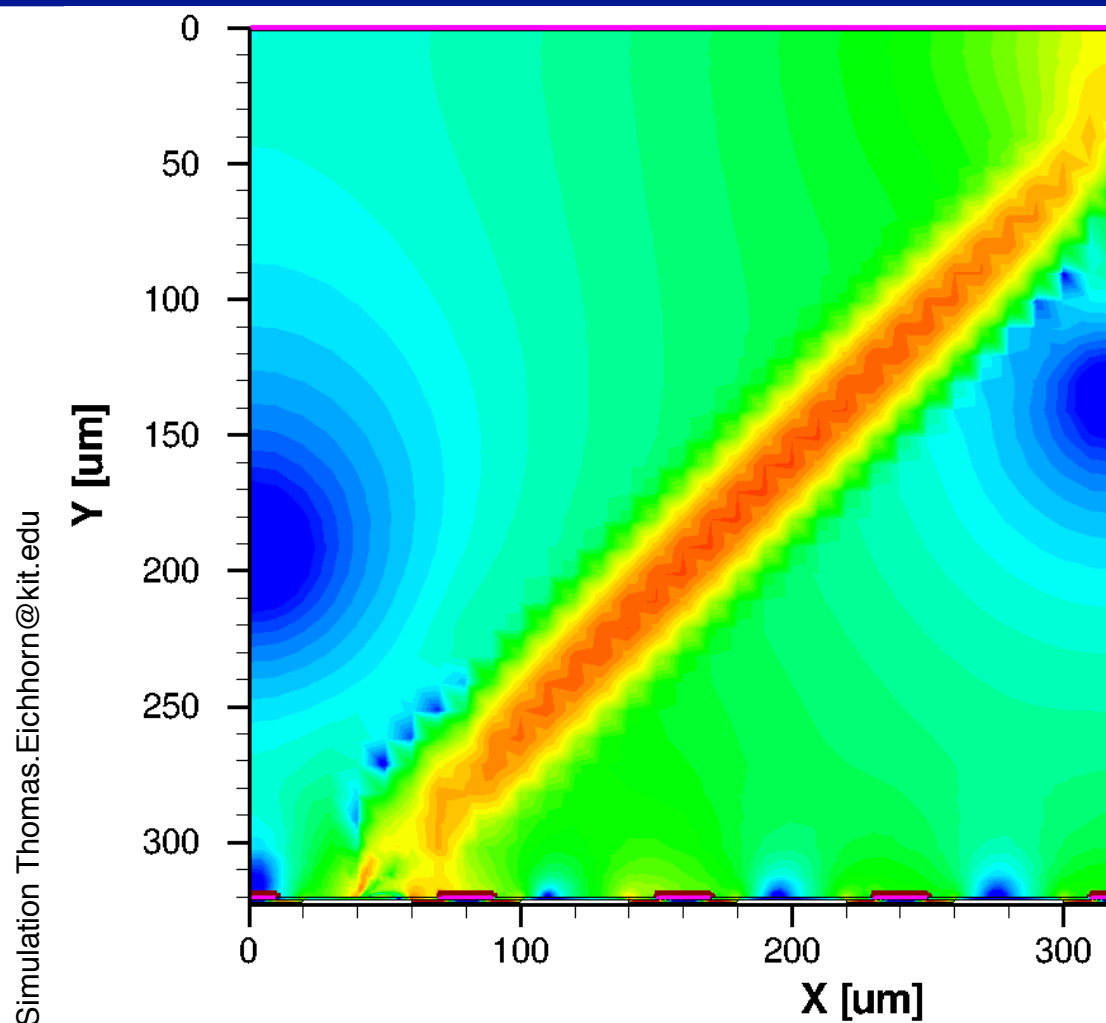
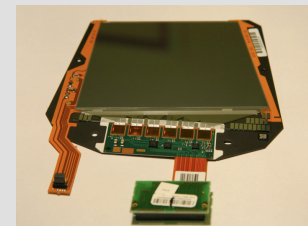


## 2.2. Simulated Current Density Ionizing particle with 45° angle t=1 ns

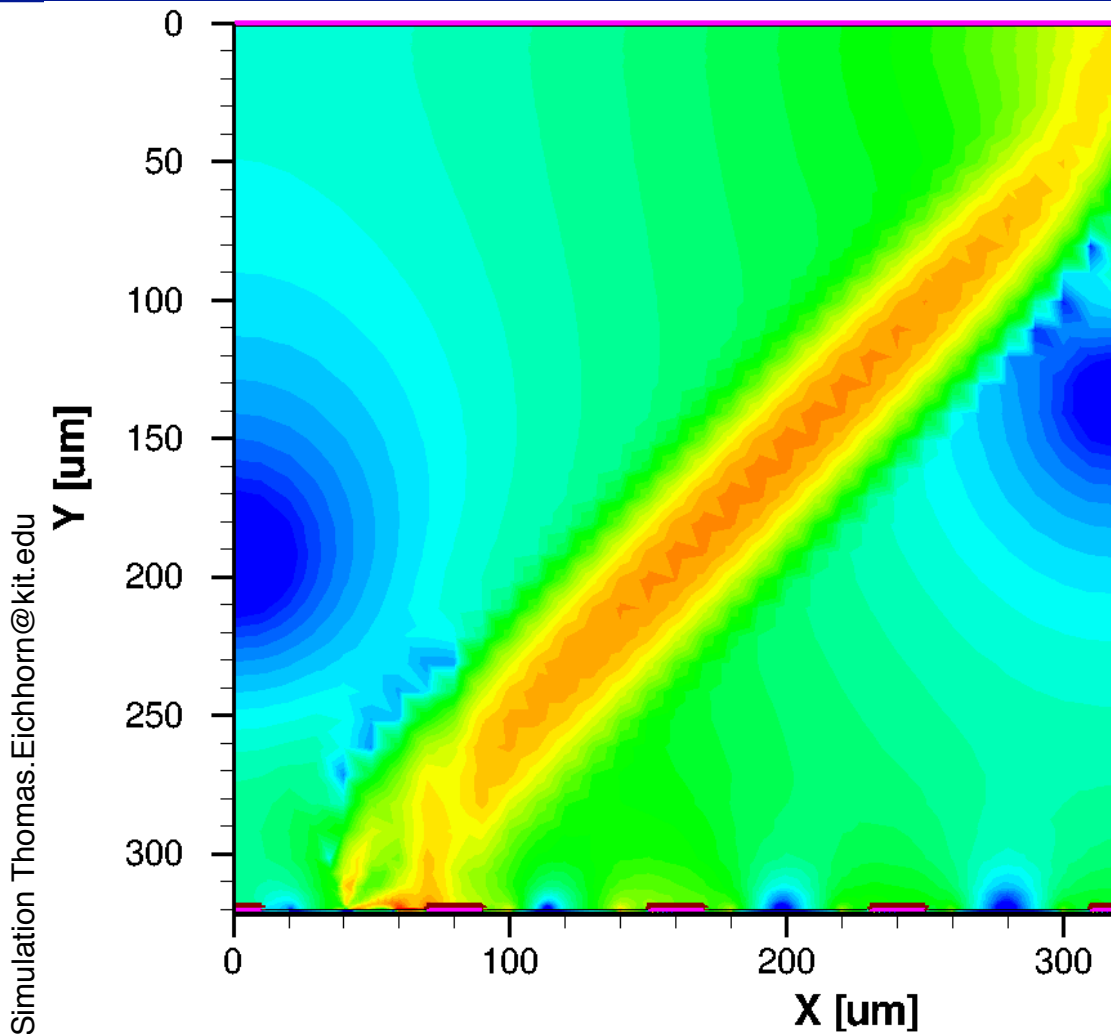
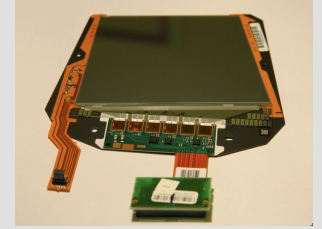


Simulation Thomas.Eichhorn@kit.edu

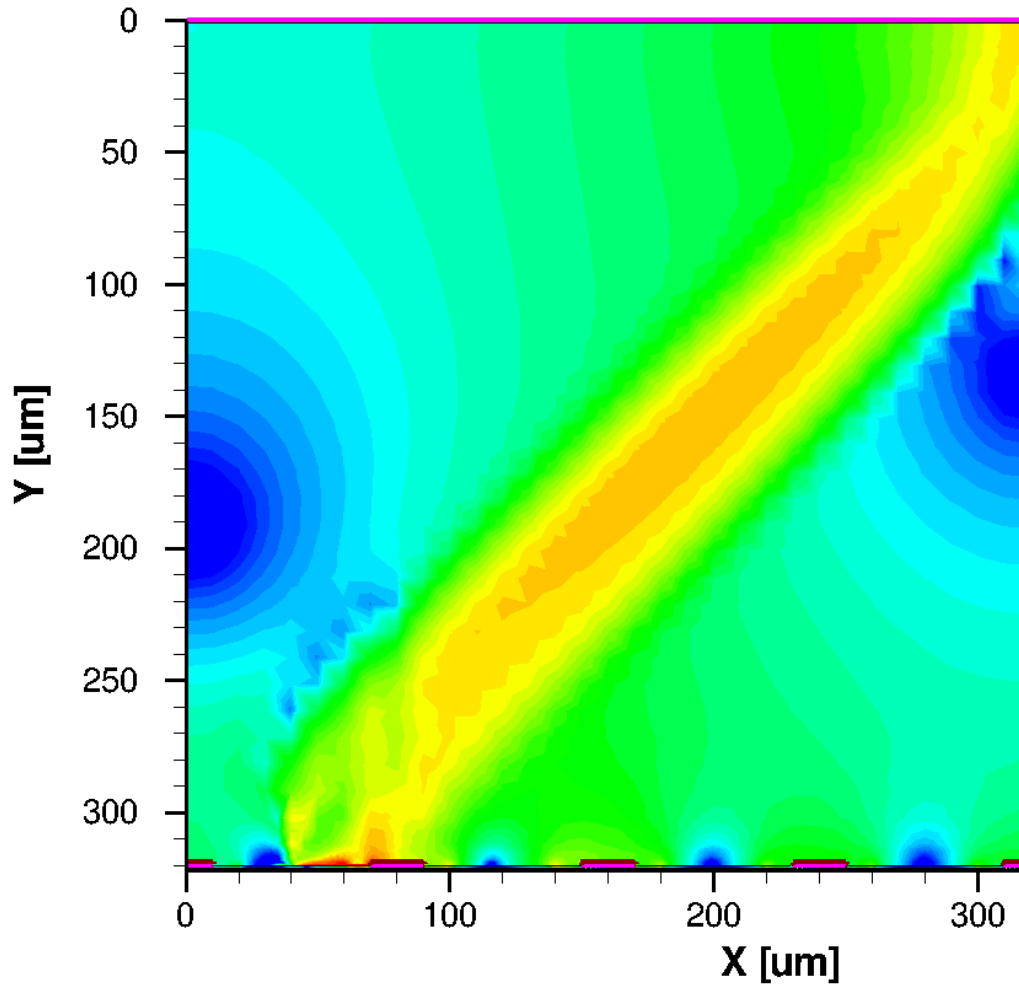
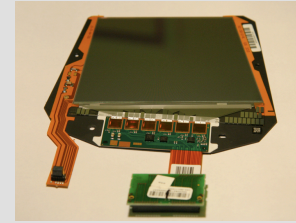
## 2.2. Simulated Current Density Ionizing particle with 45° angle t=1,1 ns



## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=1,2$ ns

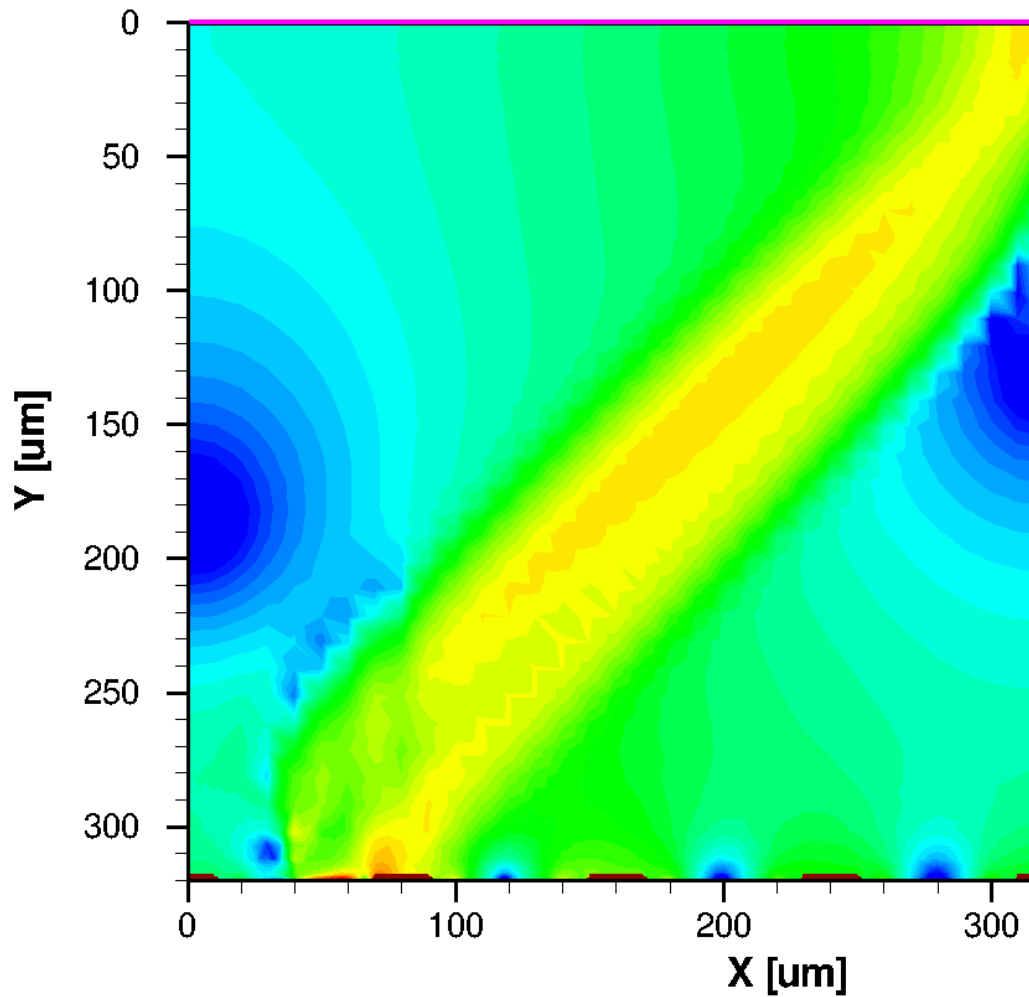
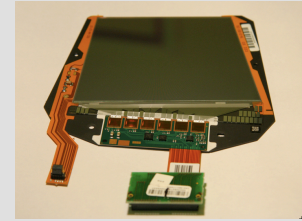


## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=1,3$ ns



Simulation Thomas.Eichhorn@kit.edu

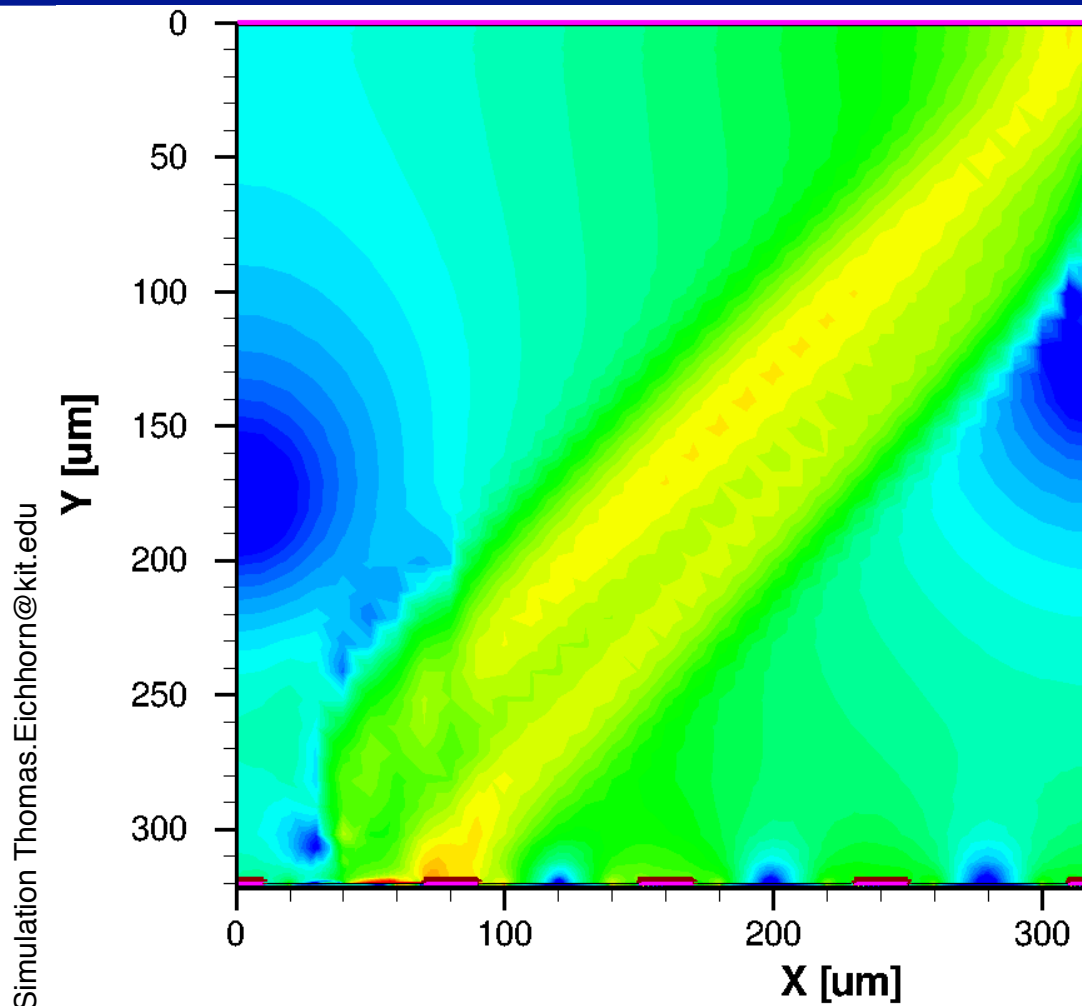
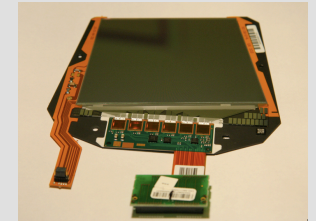
## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=1,4$ ns

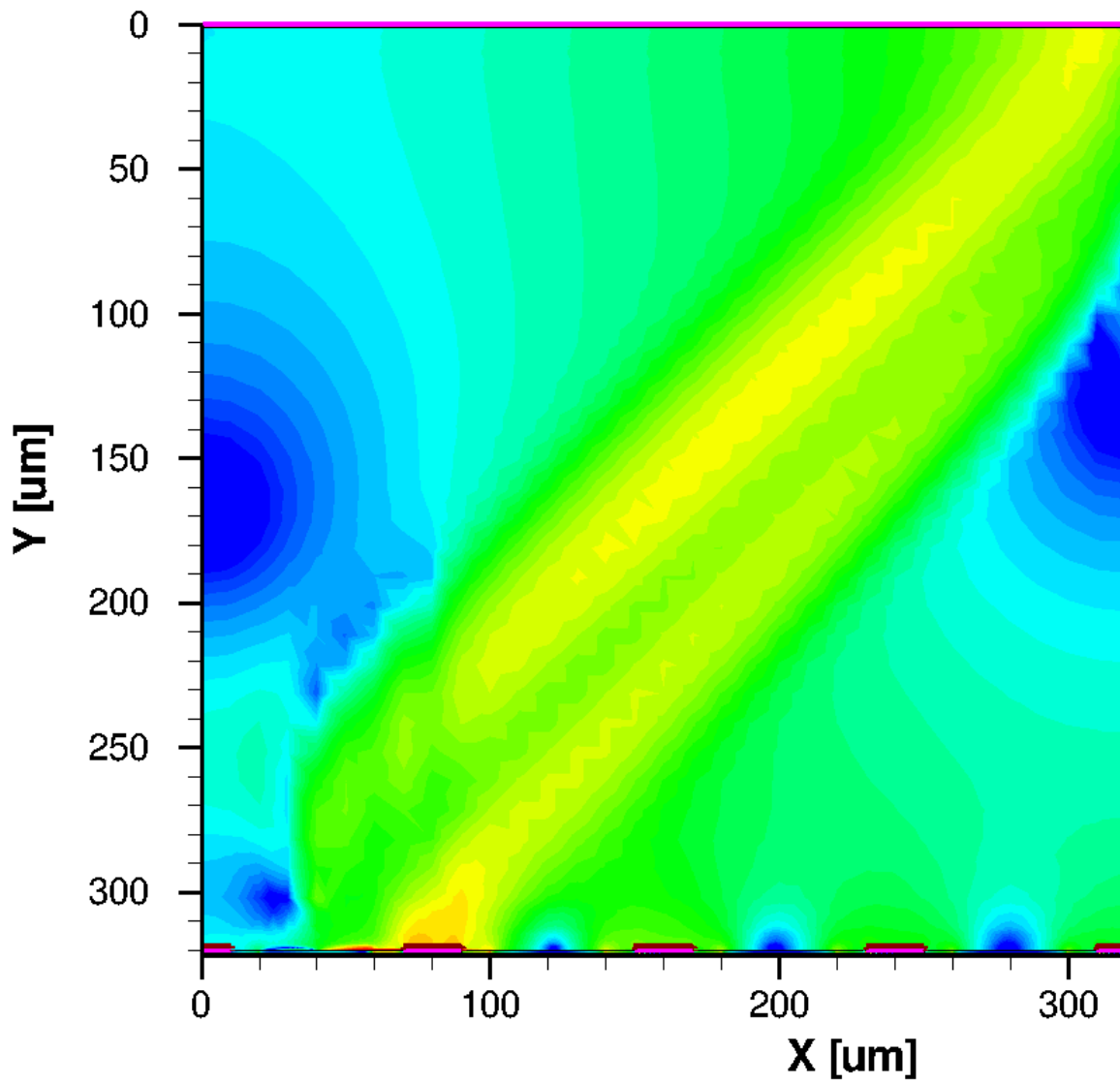


Simulation Thomas.Eichhorn@kit.edu

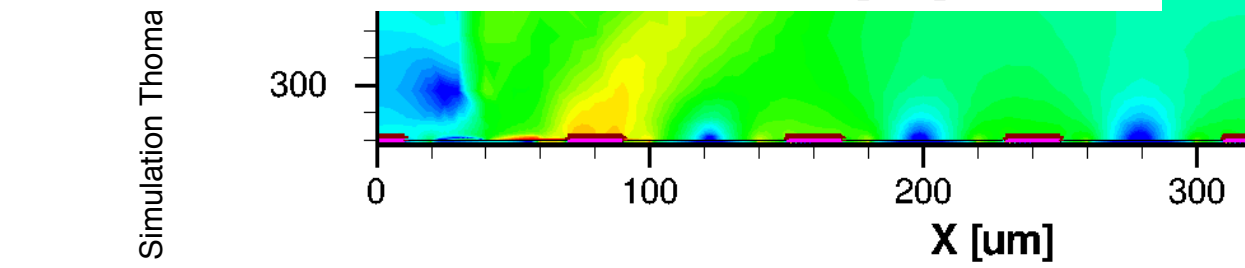


## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=1,5$ ns

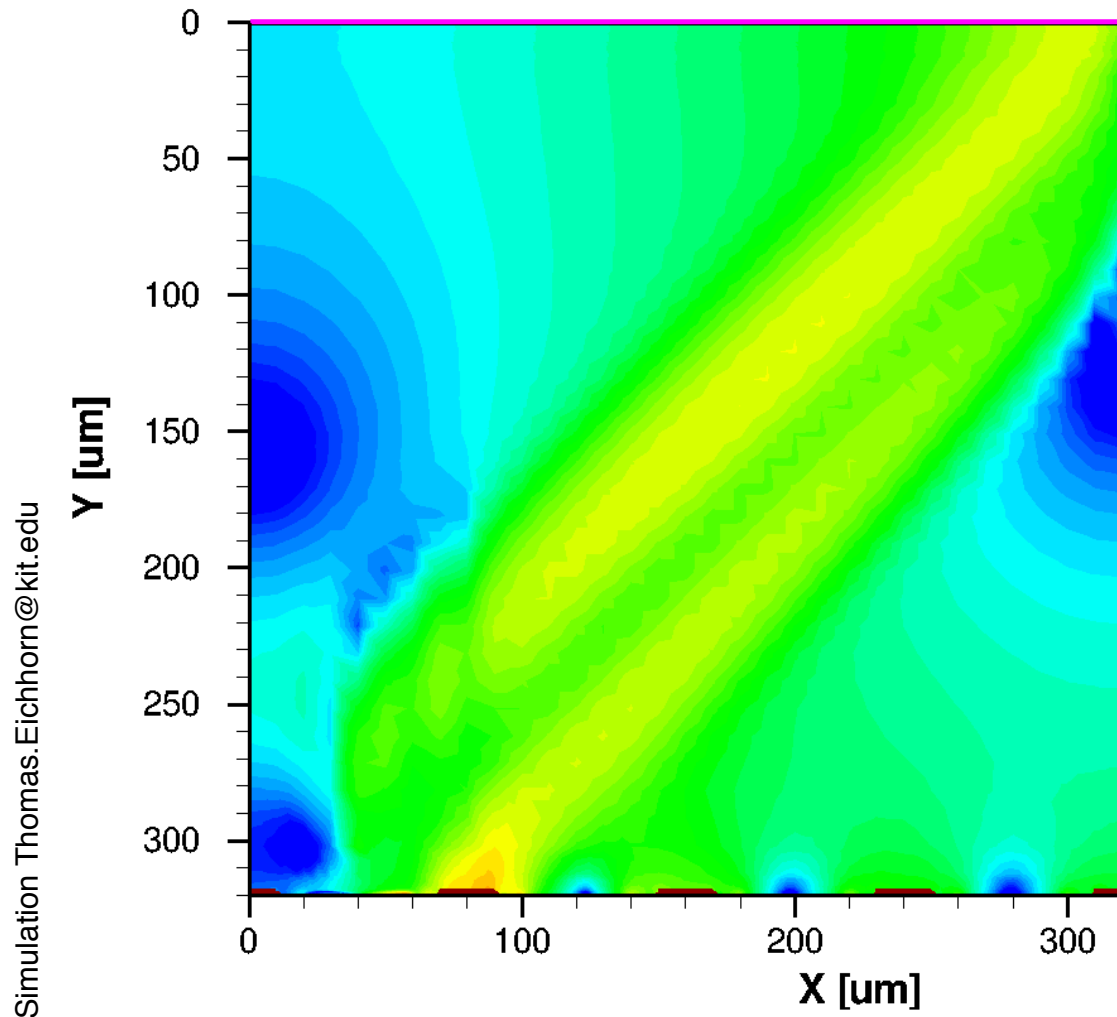
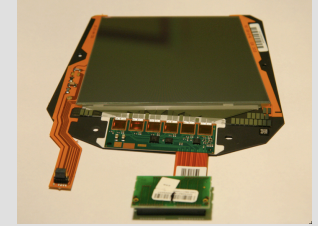




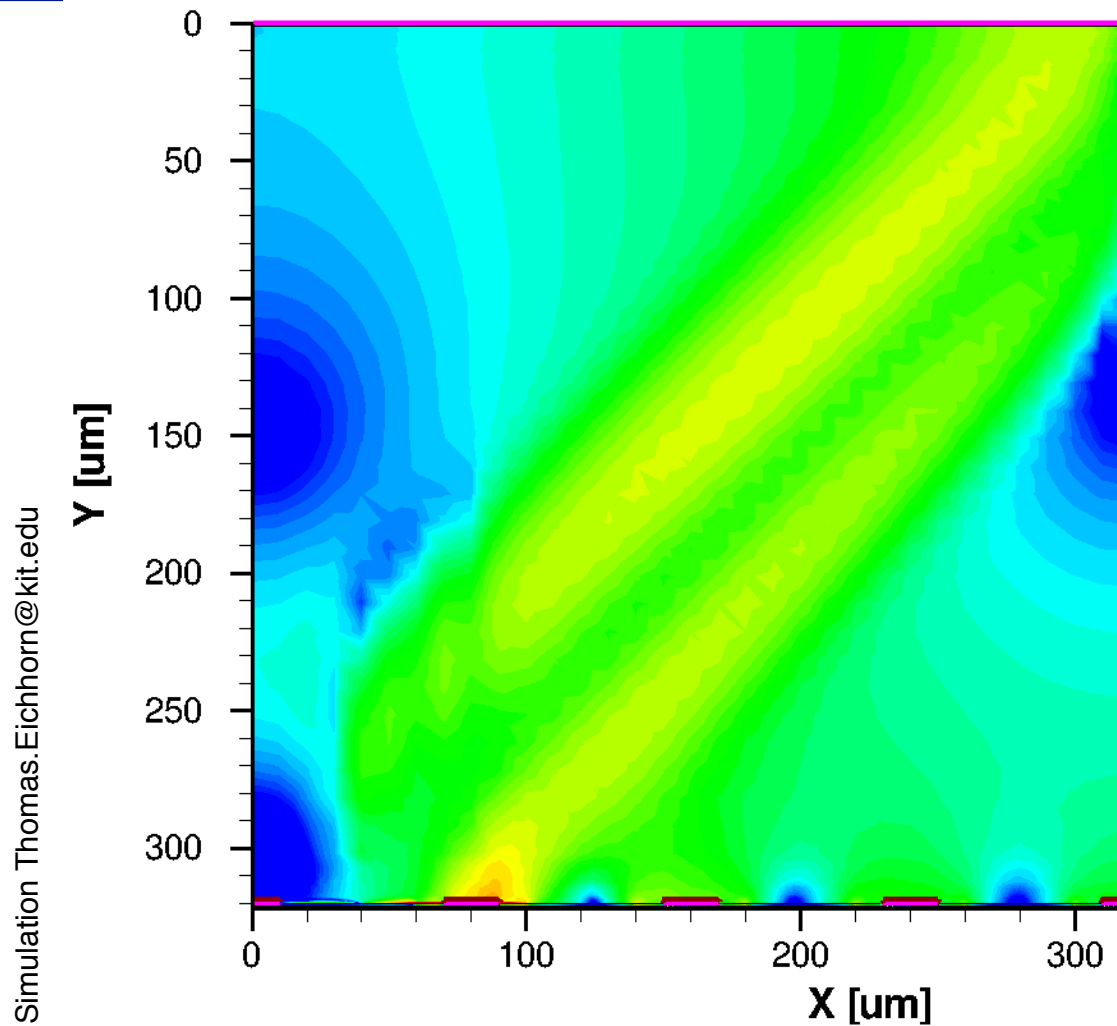
ity  
=1,6 ns



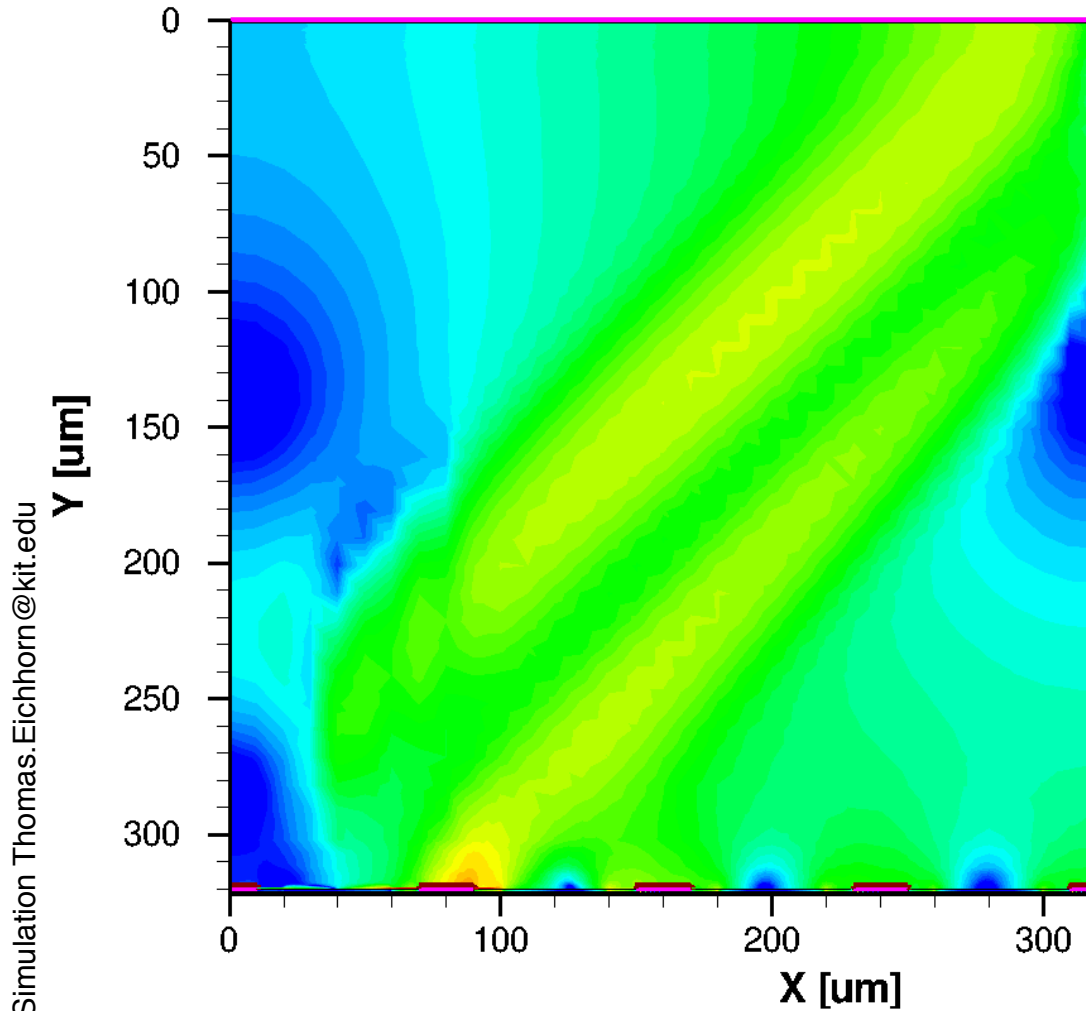
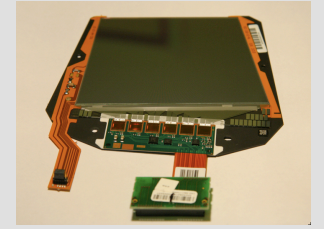
## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=1,7$ ns



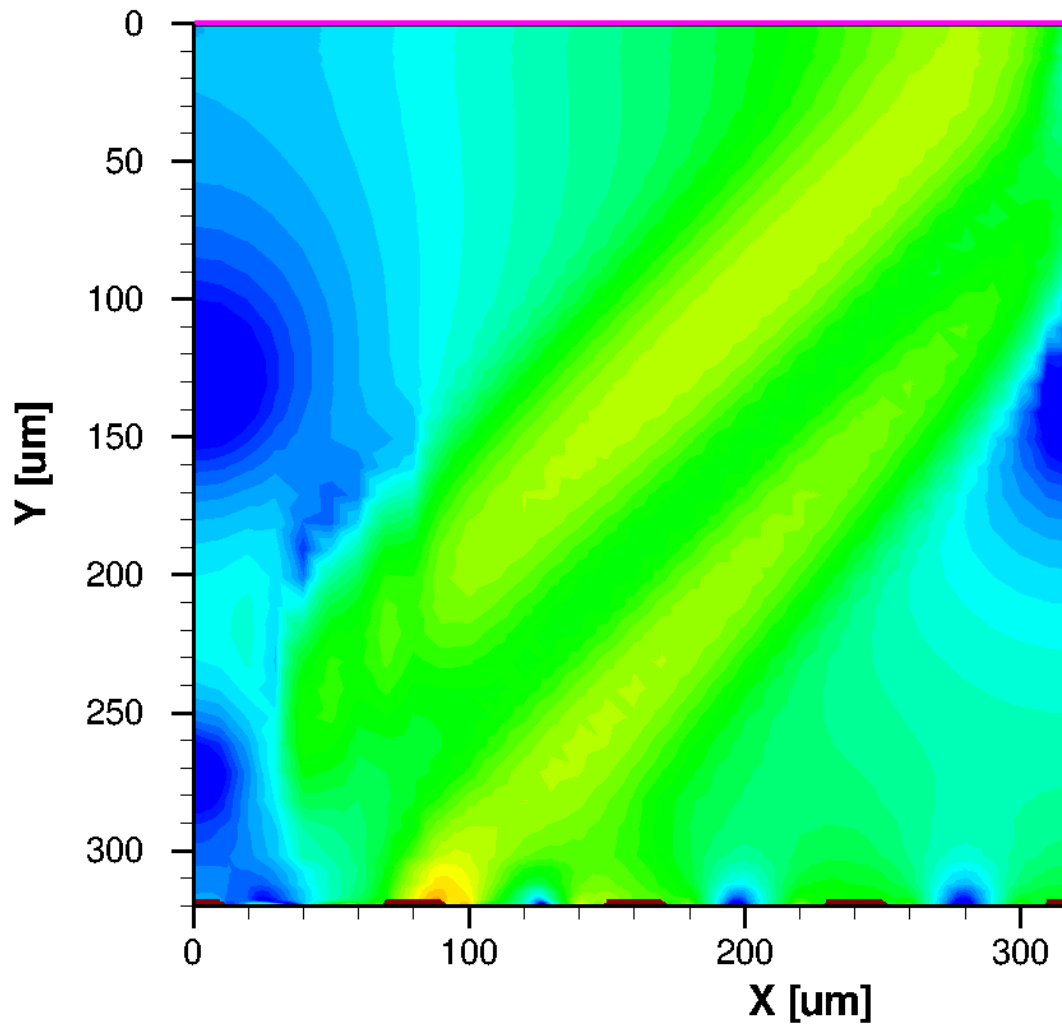
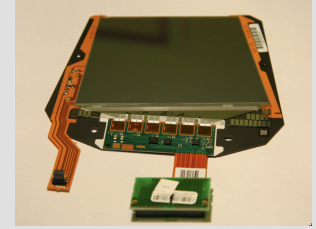
## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=1,8$ ns



## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=1,9$ ns

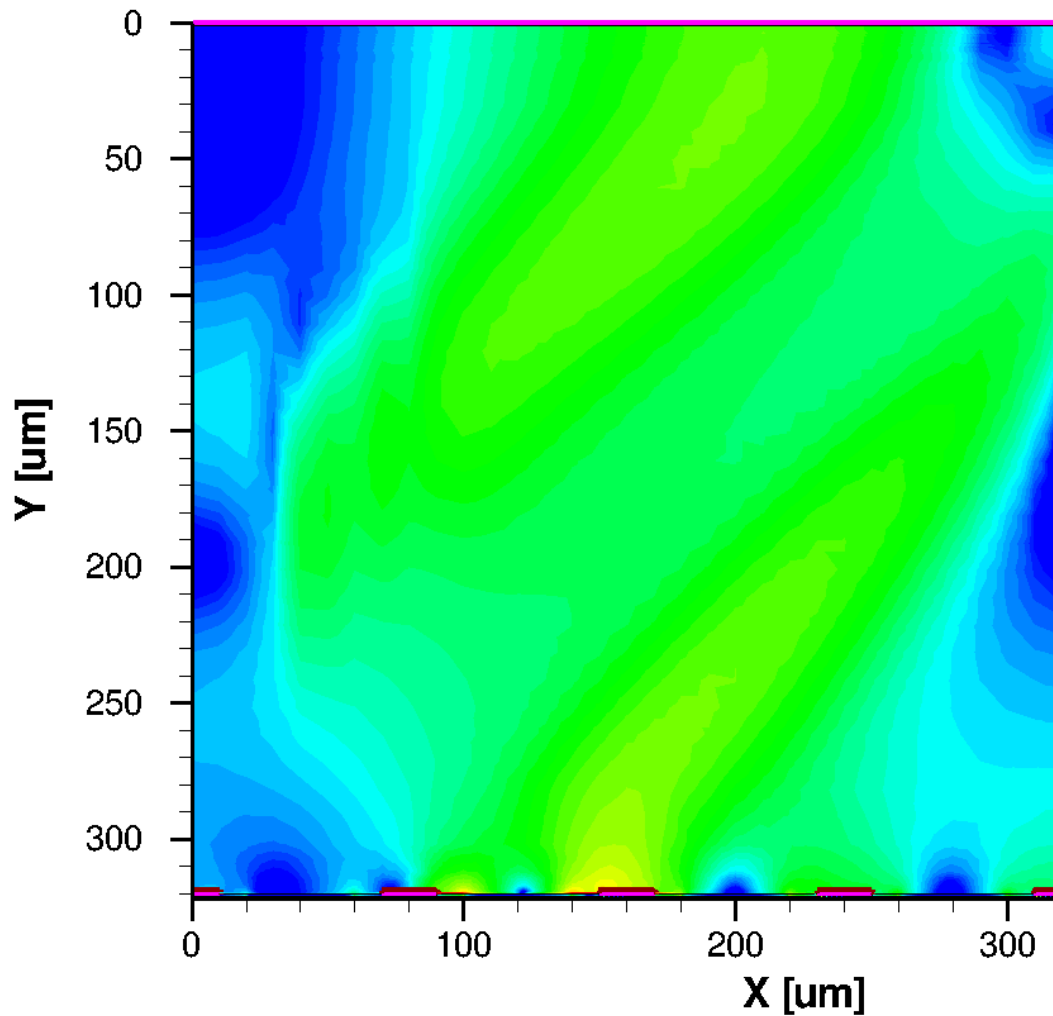


## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=2$ ns



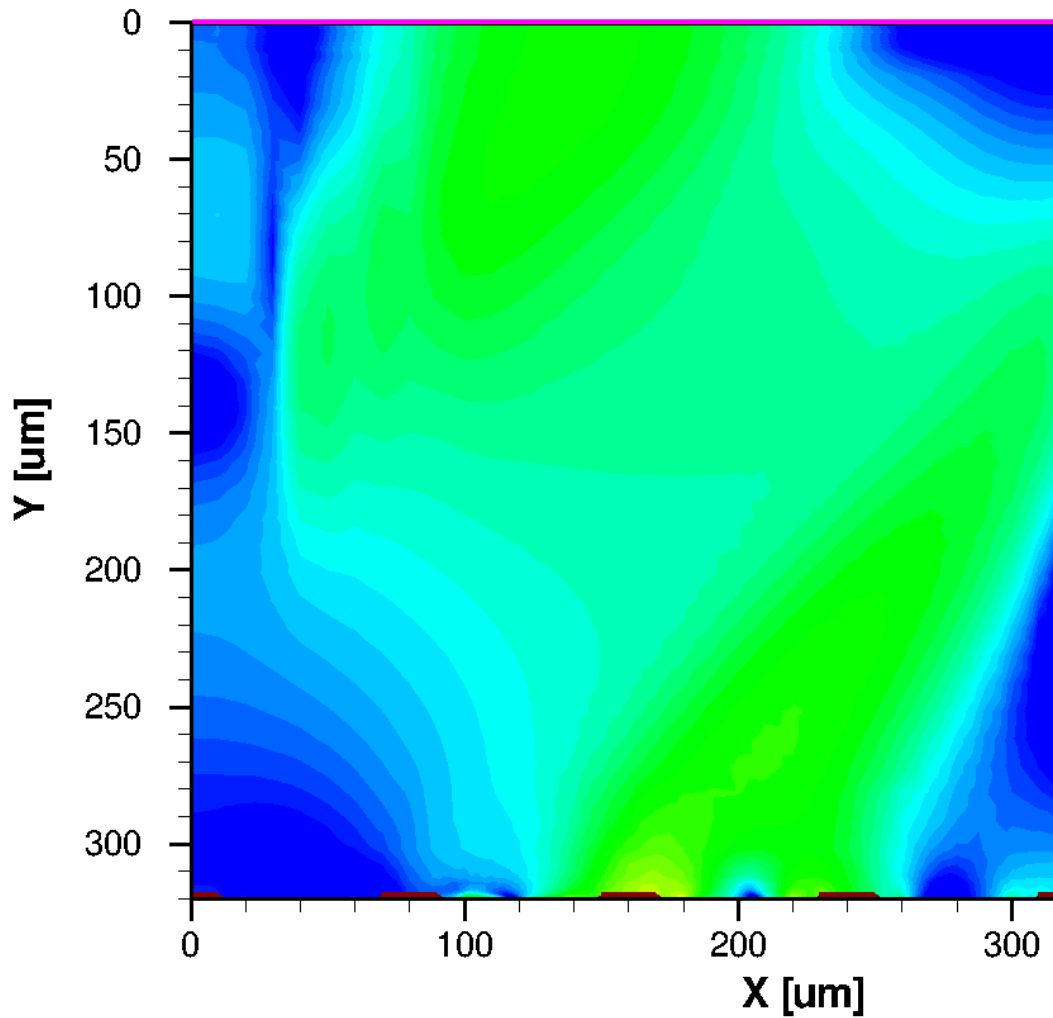
Simulation Thomas.Eichhorn@kit.edu

## 2.2. Simulated Current Density Ionizing particle with 45° angle t=3 ns



Simulation Thomas.Eichhorn@kit.edu

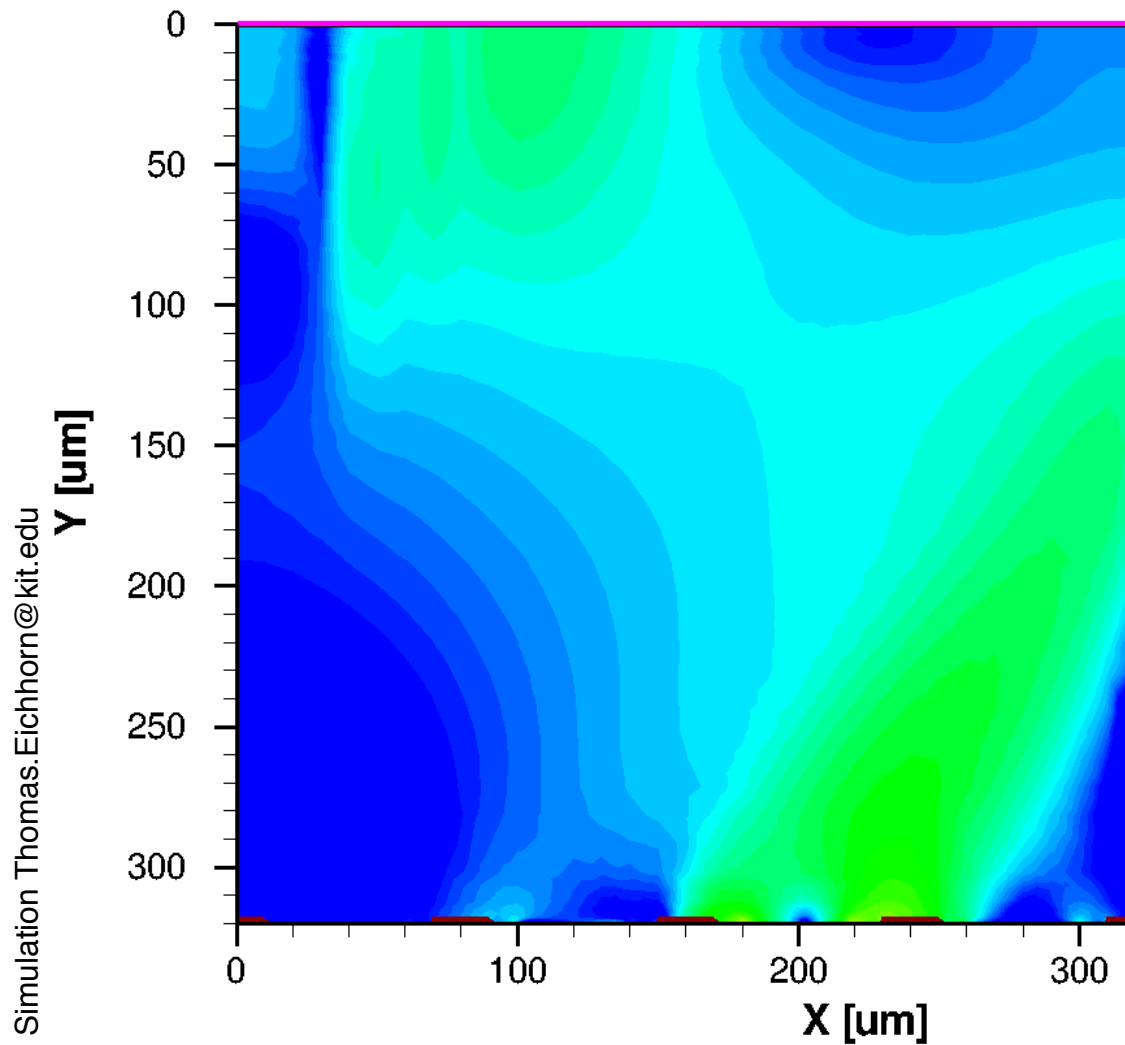
## 2.2. Simulated Current Density Ionizing particle with 45° angle $t=4$ ns



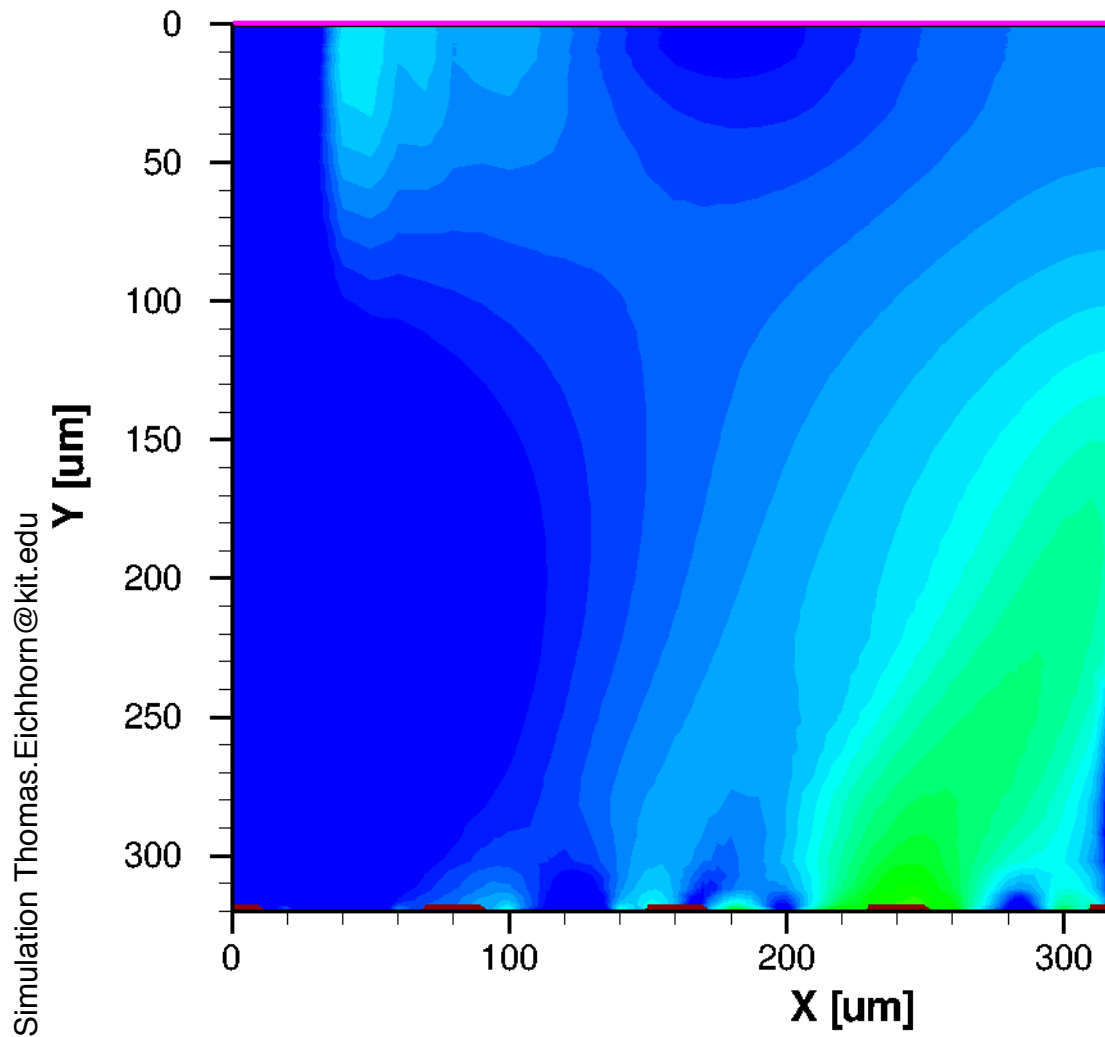
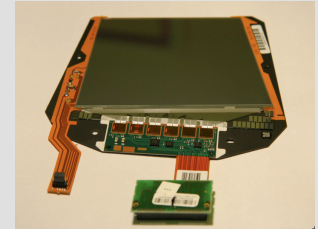
Simulation Thomas.Eichhorn@kit.edu



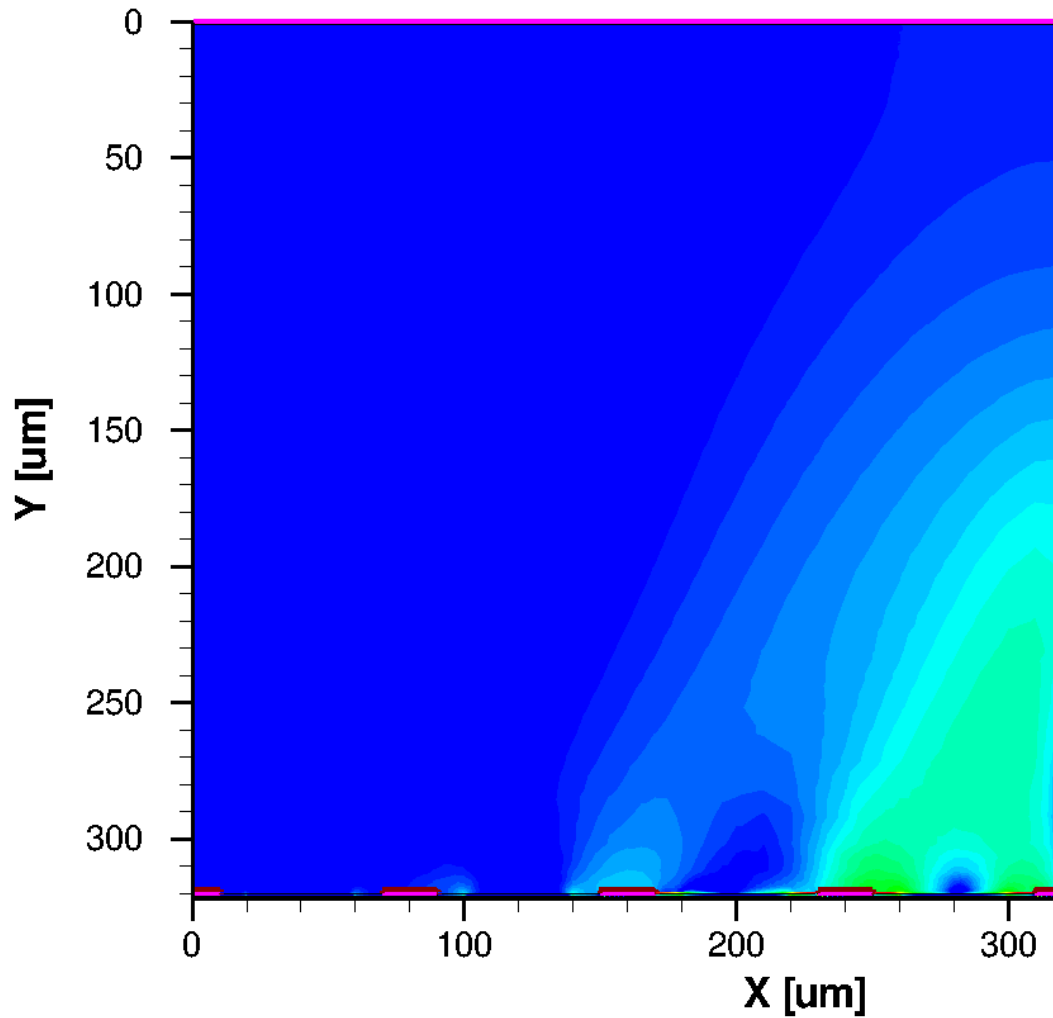
## 2.2. Simulated Current Density Ionizing particle with 45° angle t=5 ns



## 2.2. Simulated Current Density Ionizing particle with 45° angle t=6 ns



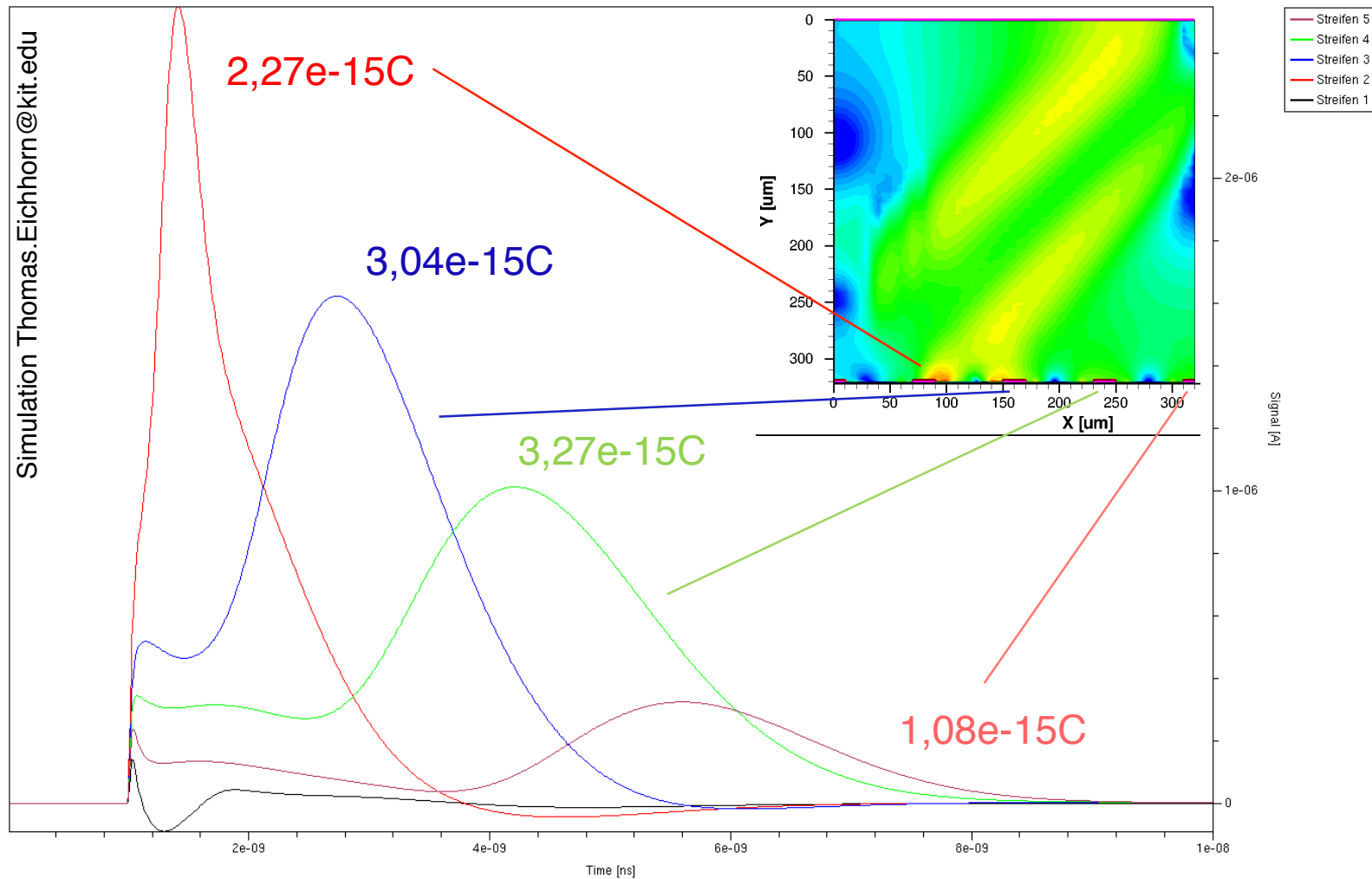
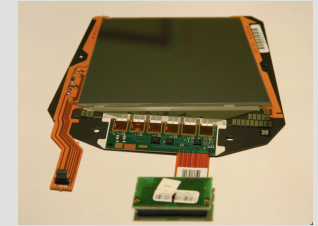
## 2.2. Simulated Current Density Ionizing particle with 45° angle t=7 ns



Mind all electrons collected

Simulation Thomas.Eichhorn@kit.edu

## 2.2. Hole Charge Collection (strip & time resolved)



# The Charge Signal

- Collected charge usually given for Minimum Ionizing Particle (MIP)

$dE/dx_{Si} = 3.88 \text{ MeV/cm}$ , for  $300 \mu\text{m}$  thick  
=  $116 \text{ keV}$

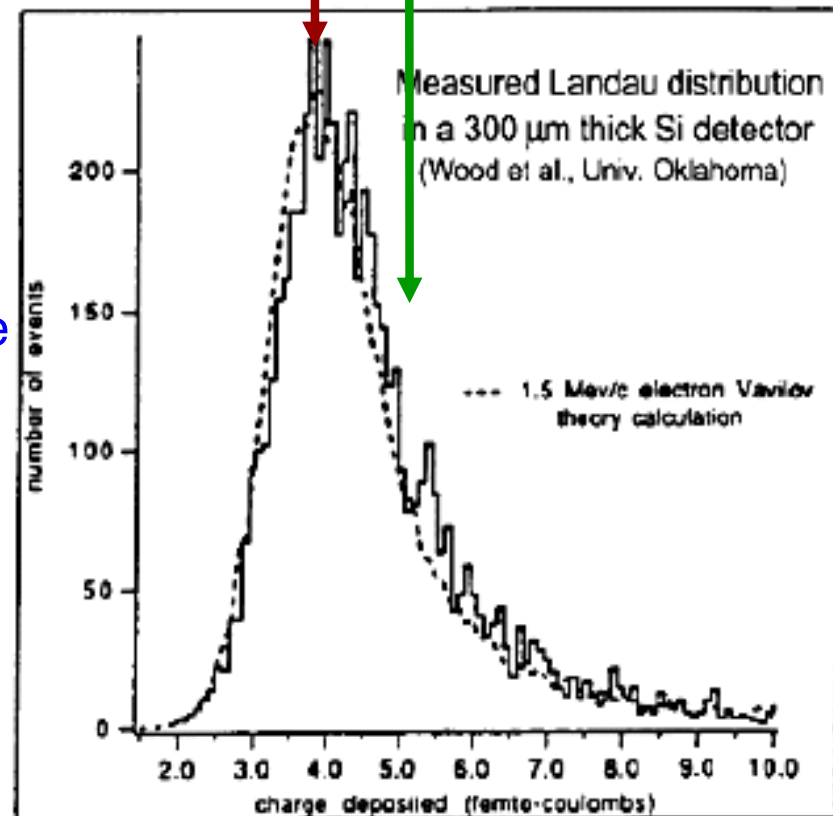
This is mean loss, for silicon detectors use  
most probable loss (0.7 mean) =  $81 \text{ keV}$

$3.6 \text{ eV}$  needed to make e-h pair

Collected charge  $22500 \text{ e}$  (=  $3.6 \text{ fC}$ )

Most probable charge  $\approx 0.7$  mean

Mean charge



## But There Is Noizzzzzz .....

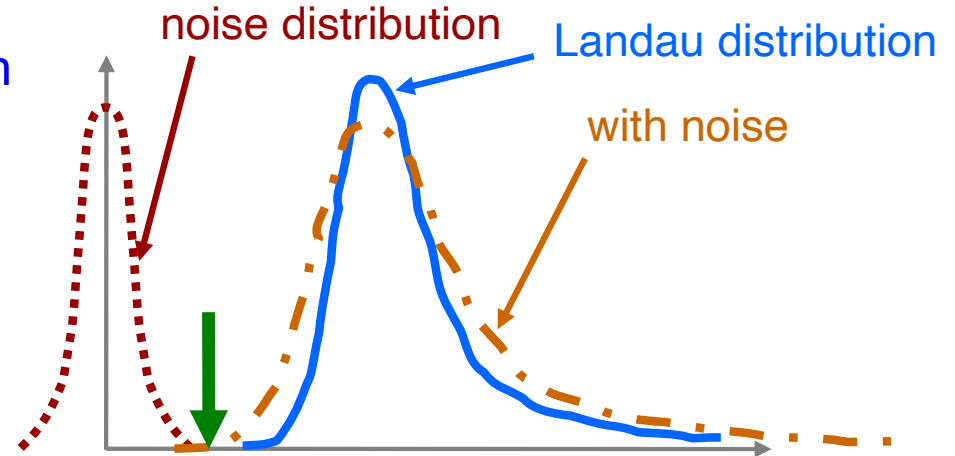
Landau distribution has a significant low energy tail which becomes even lower with noise broadening.

Noise sources (Equivalent Noise Charge):

o Capacitance ENC  $\sim C_d$

o Leakage Current ENC  $\sim \sqrt{I}$

o Thermal Noise ENC  $\sim \sqrt{(kT/R)}$



One usually has low occupancy in silicon sensors most channels have no signal. Don't want noise to produce fake hits so need to cut high above noise tail to define good hits. But if too high you lose efficiency for real signals.

Figure of Merit: **Signal-to-Noise Ratio S/N.**

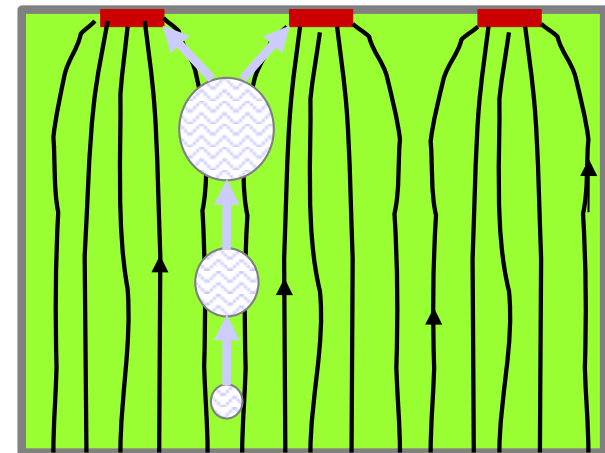
Typical Values  $\sim 10-15$ , people get nervous below 10. Radiation Damage can degrade the S/N. Thus S/N determines detector lifetime in radiation environment.

# Charge Collection and Diffusion

- Drift velocity of charge carriers  $v = \mu E$ , so drift time,  
 $t_d = d/v = d/\mu E$
- Typical values:  $d=300 \mu\text{m}$ ,  $E= 2.5\text{kV/cm}$ ,  $\mu_e= 1350$ ;  $\mu_h= 450 \text{ cm}^2 / \text{V}\cdot\text{s}$ ,  
gives:  $t_d(e)= 9\text{ns}$  ,  $t_d(h)= 27\text{ns}$
- Diffusion of charge “cloud” caused by scattering of drifting charge carriers, radius of distribution after time  $t_d$ :

$$\sigma = \sqrt{2D t_d} \quad , \text{ where } D \text{ is the diffusion constant, } D = \mu kT/q$$

- Typical charge radius:  $\approx 6 \mu\text{m}$
- Charge Radius determines ‘Charge Sharing’, i.e. deposition of charge on several strips.



# Double Sided Detectors

Why not get a 2<sup>nd</sup> coordinate by measuring position of the (electron) charge collected on the opposite face?

BUT:

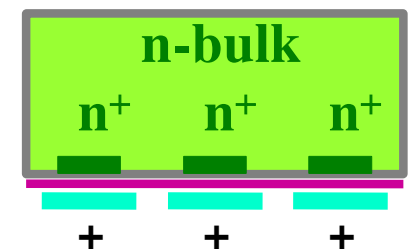
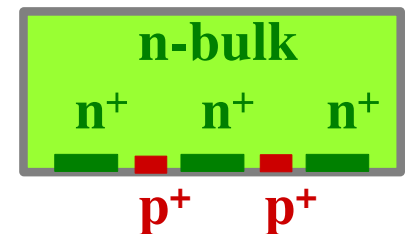
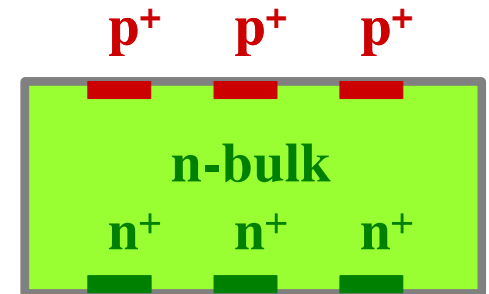
Unlike the face with the p-strips, nothing prevents horizontal charge spread on back face. n-strips alone are not sufficient to isolate the charge because of an electron accumulation layer produced by the positively charged SiO<sub>2</sub> layer on the surface.

SOLUTION:

- Put p-strips in between the n-strips.

OR

- Put “field plates” (metal over oxide) over the n-strips and apply a potential to repel the electrons.



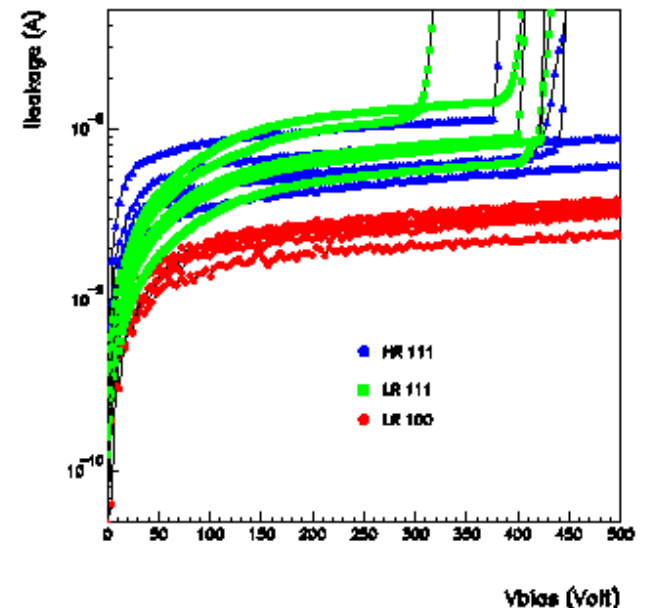
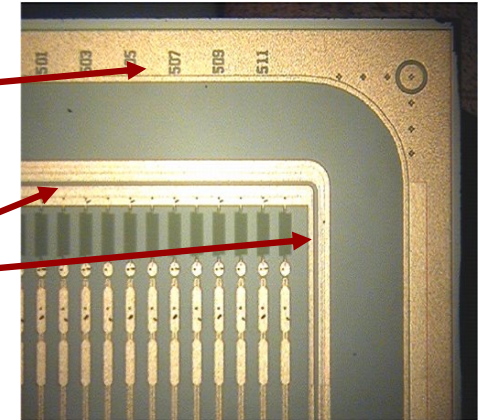


# Guard Rings and Avalanche Breakdown

We have treated the silicon strip device as having infinite area, but it has edges. What happens at the edges?

- Voltage drop between biasing ring and edge, top edge at backplane voltage.
- Typically n-type implants put around edge of the device and a proper distance maintained between p bias ring and edge ring.
- Usually one or more “guard” rings (left floating) to assure continuous potential drop over this region.
- Defects or oxide charge build-up in this region could lead to additional leakage current contributions
- If one increases the bias voltage, eventually the field is high enough to initiate avalanche multiplication. This usually occurs around  $30\text{V}/\mu\text{m}$  (compared to a typical operating field of  $<1\text{V}/\mu\text{m}$ ). Local defects and inhomogeneities could result in fields approaching the breakdown point.

Single guard ring structure



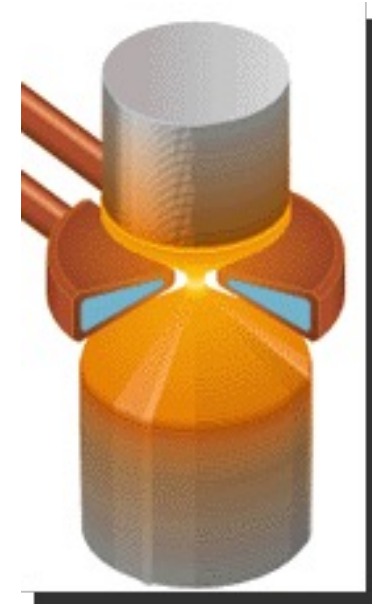
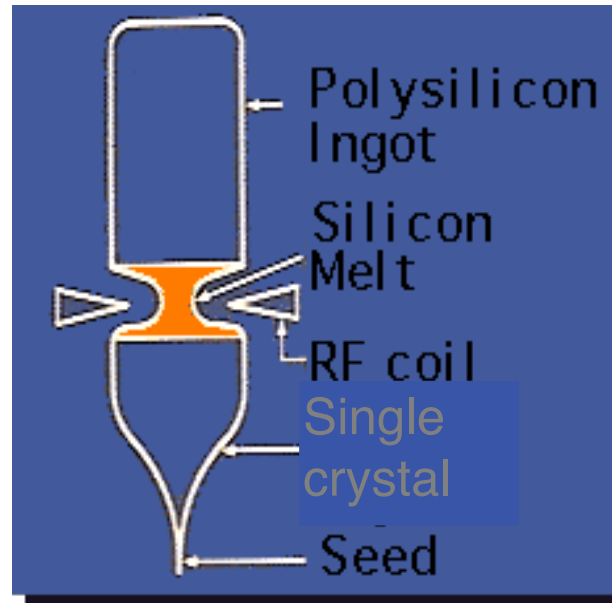
## Some Technicalities .....

# Wafer Fabrication

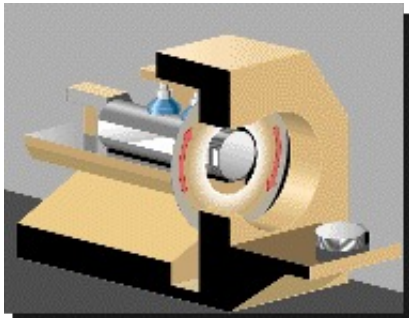
1) Start with very pure quartzite sand from your nearest beach and clean and further purify by chemical processes. Melt, and add the tiny concentration of phosphorus (boron) dopant to make n(p) type silicon. Pour in mold to make a polycrystalline silicon cylinder.



2) Using a single silicon crystal seed, melt the vertically oriented cylinder onto the seed using RF power to obtain single crystal 'ingot'.



3) Slice ingot into wafers of thickness  $300\ \mu\text{m}$  to  $500\ \mu\text{m}$  with diamond encrusted wire or disc saws.




20/5/2004

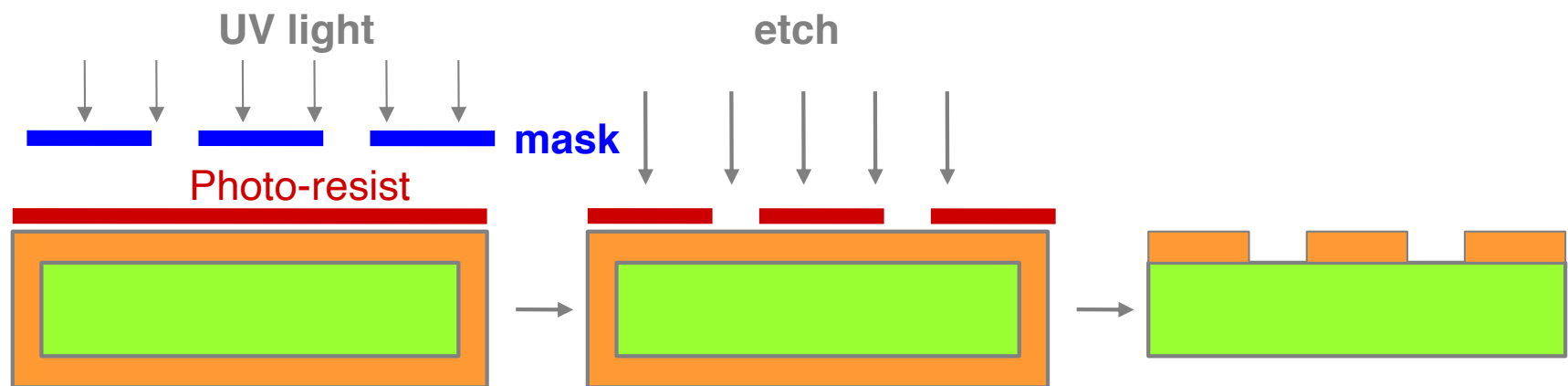
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# Wafer Processing (1)

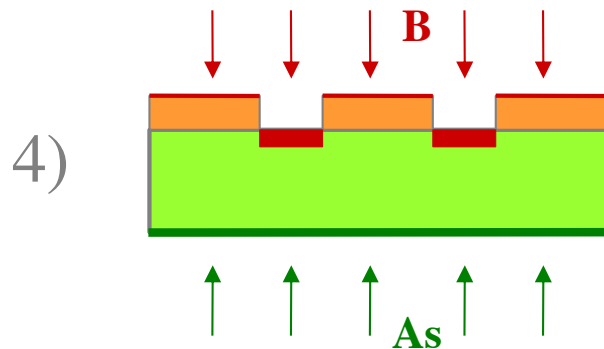
1)  **n-Si** Start with n-doped silicon wafer,  $\rho \approx 1-10 \text{ k}\Omega\text{cm}$

2)  **SiO<sub>2</sub>** Oxidation at 800 - 1200C

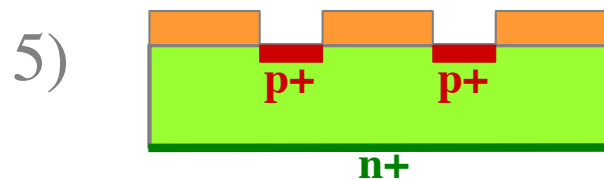
3) Photolithography (= mask align + photo-resist layer + developing) followed by etching to make windows in oxide



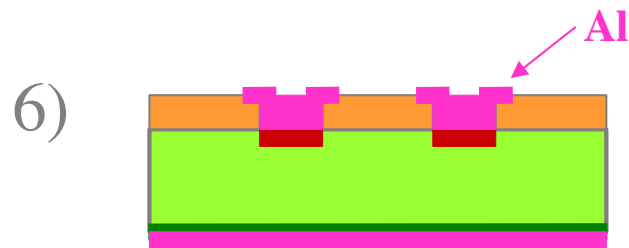
## Wafer Processing (2)



Doping by ion implantation (or by diffusion)



Annealing (healing of crystal lattice) at 600 C

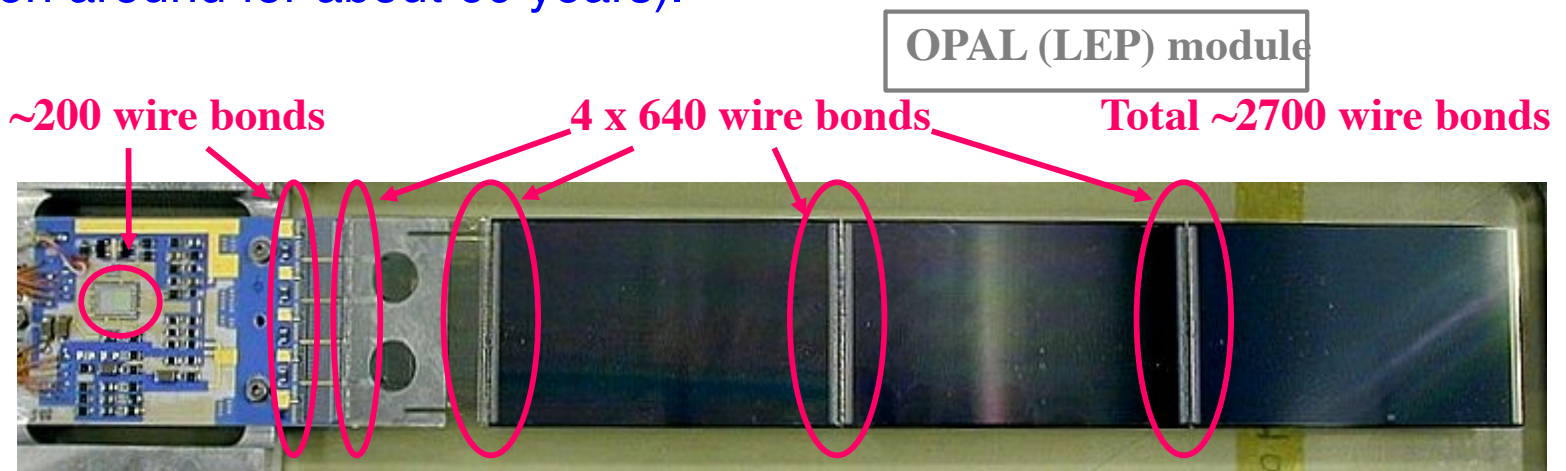


Photolithography followed by Al metallization over implanted strips and over backplane usually by evaporation.

⇒ Simple DC-coupled silicon strip detector

# Bringing It All Together

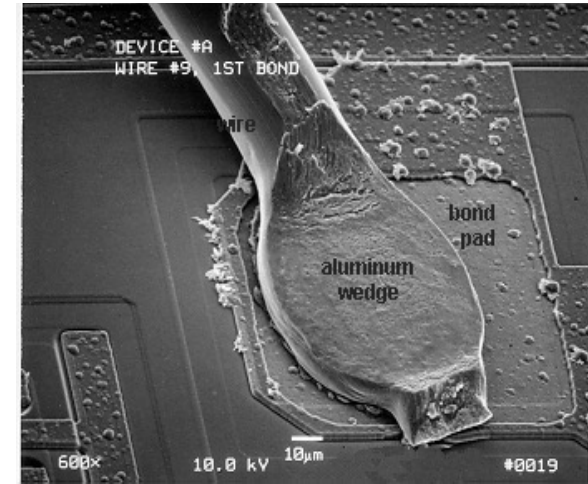
- Connectivity technology: some of the possibilities
  - High density interconnects (HDI): industry standard and custom cables, usually flexible kapton/copper with miniature connectors.
  - Soldering still standard for surface mount components, packaged chips and some cables. Conductive adhesives are often a viable low temperature alternative, especially for delicate substrates.
  - Wire bonding: the standard method for connecting sensors to each other and to the front-end chips. Usually employed for all connections of the front-end chips and bare die ASICs. A “mature” technology (has been around for about 60 years).



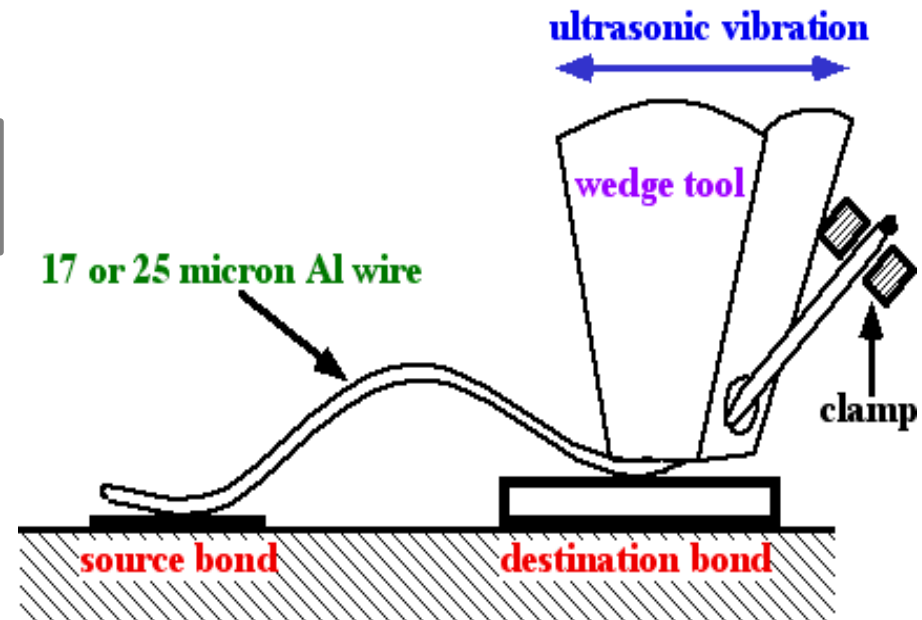
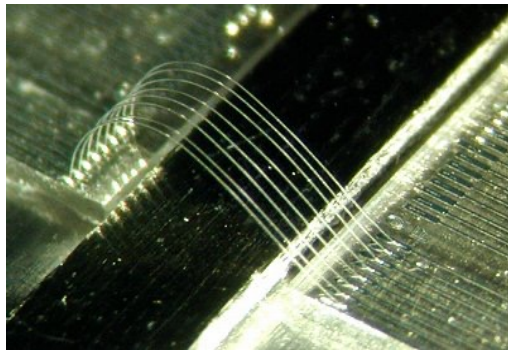
# Wire Bonding

- Uses ultrasonic power to vibrate needle-like tool on top of wire. Friction welds wire to metallized substrate underneath.
- Can easily handle 80 $\mu\text{m}$  pitch in a single row and 40 $\mu\text{m}$  in two staggered rows (typical FE chip input pitch is 44 $\mu\text{m}$ ).
- Generally use 25 $\mu\text{m}$  diameter aluminium wire and bond to aluminium pads (chips) or gold pads (hybrid substrates).
- Heavily used in industry (PC processors) but not with such thin wire or small pitch.

Electron micrograph of bond “foot”



Microscope view of wire bonds connecting sensor to fan-out circuit



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# Summary

Silicon strip detectors built on simple pn junction principle have become a 'mature' technology in little more than 20 years.

Provide reliable tracking in high density/high rate environment

Widespread use thanks to cost drop and advances in microelectronic industry

## Have **not** covered:

- CDF Silicon IIa, IIb =>
- Radiation Damage =>
- Role of readout electronics
- Alternatives to Silicon (Ge, Diamond ...)
- Silicon Detectors based on pixels, pads, Silicon Drift Chambers etc.
- .....