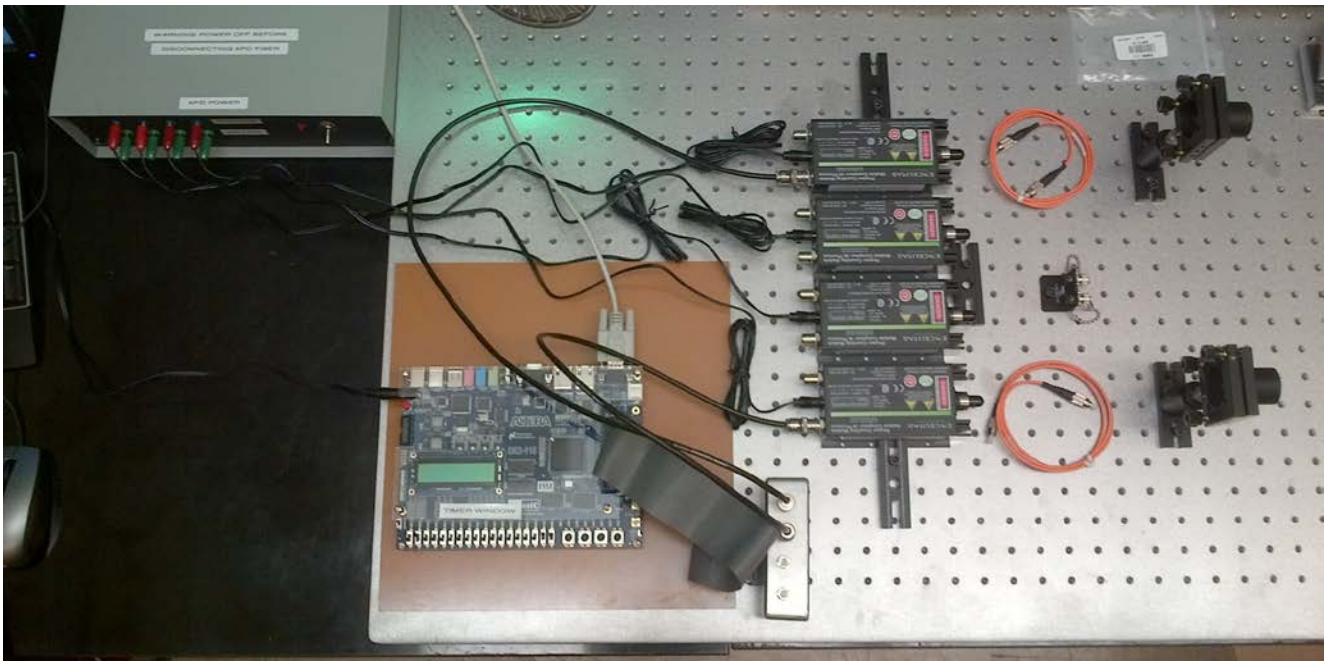
Final Design:
Single Photon Detector Experiment

Client: University of Toronto Advanced Physics Laboratory



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1 Executive Summary

The final design of a detection module for a future quantum entanglement experiment in the Undergraduate Advanced Physics Lab at the University of Toronto is presented. The experiment is located in Room 244 of the McLennan Physics building. Four avalanche photo diode single-photon detectors are used to detect incident photons and transmit signals to a DE2-115 Development Board for photon coincidence determination. The signals are transmitted via BNC cables through a BNC to 40-pin cable Hub. The logic implemented on the FPGA of the DE2-115 utilizes LCELLs to shorten incident pulses and create coincidence detection windows. AND-gate logic is then used to calculate coincidences and store both coincidences and single counts in onboard registers. The DE2-115 communicates this register data over an RS232 connection to a LabVIEW equipped PC computer in 0.1 second intervals. A LabVIEW program is designed to display the single and coincidence detection data through a user friendly interface and is capable of applying statistical error correction to filter classical "accidentals" from the coincidence results. Operating protocols as well as five experiments to test system functionality were also developed. The design of each component has been performed with utmost consideration for the requirements of the client, Professor David Bailey, as well as the stakeholders, objectives, constraints and metrics outlined in the project proposal [1] and preliminary design [2].

2 Problem Statement

The Undergraduate Advanced Physics Lab at the University of Toronto is looking to introduce an apparatus capable of experimentally testing the predictions of quantum mechanics using entangled photons. It will serve the purpose of adding to the educational experience of students by allowing undergraduates in both Physics and Engineering Science to directly observe quantum mechanical phenomena taught to them in their other undergraduate courses. The primary goal of the first phase of the completed experiment is to test the well-known Bell's Inequality thus showing that quantum mechanics cannot be explained by a local hidden variable theory.

Professor David C. Bailey, coordinator of the advanced lab at UofT, has requested for the design of the photon detector module of the experiment. The purpose of the detector module is to detect when two photons form a quantum entangled pair and then record the detection event. The entangled pairs are expected to be created by parametric down conversion earlier in the apparatus pipeline. If one photon is sent into the down conversion crystal and then two photons are detected at its output, it is inferred that these two photons form an entangled pair. The detection module is able to perform coincident photon detection on up to four detectors and record quantum entangled photon events between all combinations of detectors. As the laboratory is intended for undergraduate students, it has been designed to be simple, safe, and relatively cost-effective. The design has been largely based upon reference solutions from advanced physics labs that have been compared and contrasted in the preliminary design document [2]. Concurrently, significant design consideration has been given to the specific

needs of the stakeholders at the University of Toronto Undergraduate Advanced Physics Laboratory: users, lab administrators and course administrators.

3 Design Description

The completed detection module is shown in Figure 1. It is used to register and interpret single and coincidence photon detection events relevant for future experiments. Single photon detection is performed when photons are incident on any of the four Avalanche Photodiodes (APDs). If photons arrive at the detectors within a specified coincidence window of time $(3ns - 20ns)$ then they are considered coincident. Coincidence counting calculations are performed by hardware logic on a DE2-115 Field-Programmable Gate Array (FPGA) which passes all coincidence and count information to a computer. The single detection counts, coincident detection counts and statistical counting errors are then reported to the user through a LabVIEW interface on the computer.

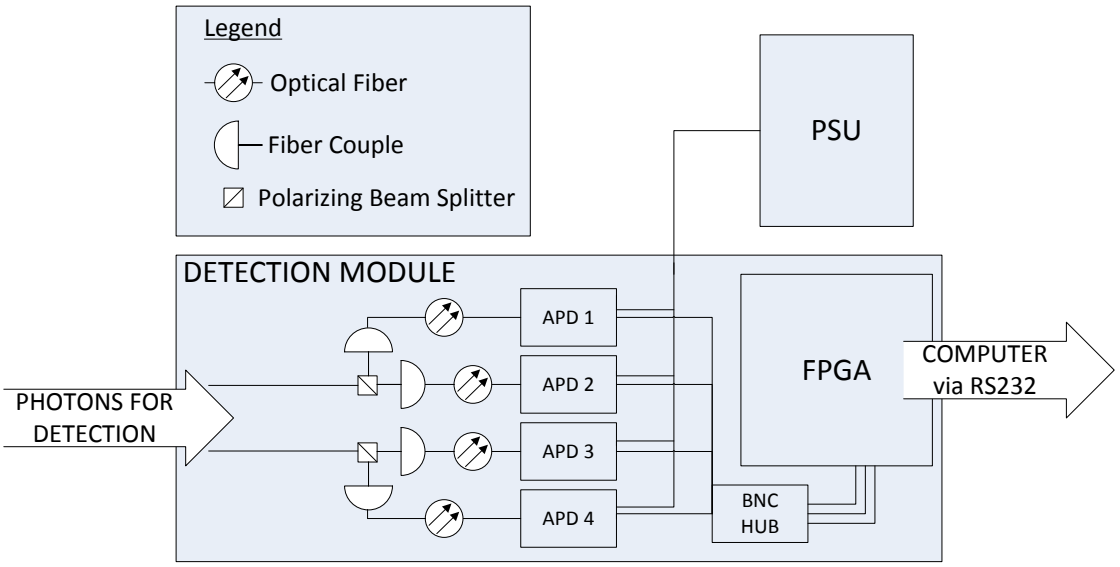


Figure 1 - Overview of the Detection Module

Components:

- FPGA: DE2-115
- APDs: Excelitas SPCM-EDU CD3375H22332
- PSU: +5V/1.2A(per plug) Power Supply Unit
- BNC Cable to 40-Pin Parallel Cable Connection HUB
- <3dB Multimode Fiber Optic Cables
- Fiber Coupling Stages, each contain:
    - 2x 1” Lens Tubes
    - Aspherical Coupling Lens (C220TME-B f=11.00mm)
    - Aperture Iris Shutter
    - Kinematic Table Mount

The design of the detection module is divided into three major design components: electromechanical design, FPGA logic design, and LabVIEW design. The following sections will give an overview for the final design for each component. For operating protocols please see the document “Walkthrough_Final.docx” located in the desktop folder “Detection” of the lab computer in MP244.

3.1 Electromechanical Design

The electromechanical component of the detection module design has been divided into four further sub-modules: physical layout of the lab room and the optical bench, power supply for the APDs, DE2-115 circuit housing and APD to DE2-115 connection HUB. The following is a detailed description of the design of each sub-module and the APDs.

Physical Layout

The physical apparatus has been constructed in-place in the McLennan physics building in Room 244 of the Advanced Physics Laboratory (Figure 2). The room contains the quantum entanglement experiment as well as general purpose storage space. The room layout has been chosen to protect students from the future planned bench-top class 3B laser and limit student access to sensitive components relative to the detection module. It will also increase access to the future experiment module and allow sufficient space for the student to work comfortably on the LabVIEW equipped PC while taking handwritten notes in their lab notebook. It was anticipated that the laser will be positioned facing away from the room entrance door and be encased in accordance with UofT laser safety specifications [3].

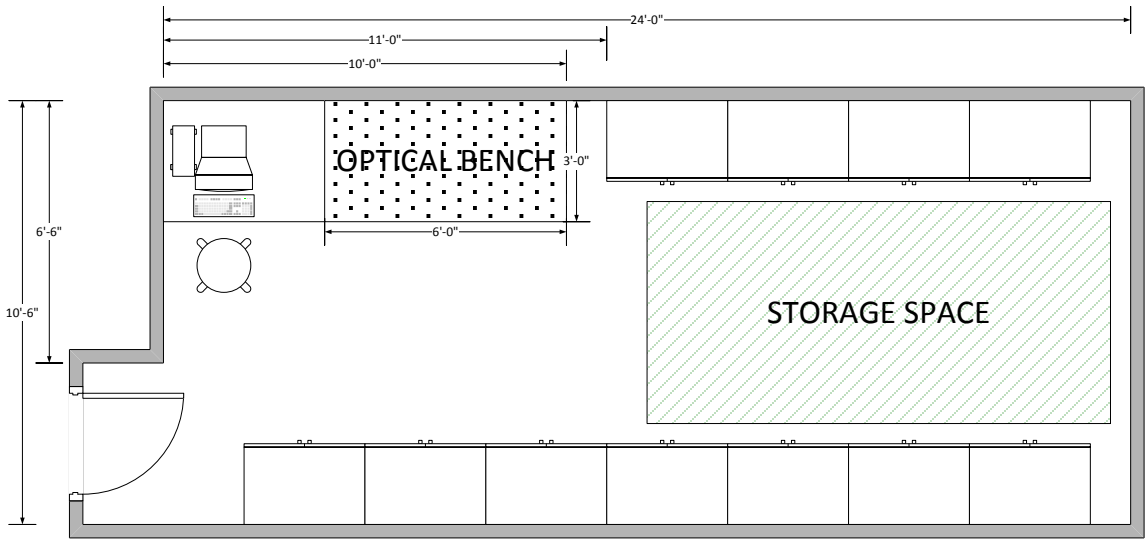


Figure 2: Room Design Layout

Optical Bench Layout

The detection module has been constructed in the lower left quadrant of the optical table and is outlined in Figure 3. The position and layout of the future experiment and generation

modules was anticipated to be similar to what has been implemented by the Steinberg Group in their Quantum Entanglement lab here at UofT [4]. However, consideration was also taken to allow flexibility for future designs. The mounting of the detection module optical components is done using non-permanent table clamps and may be easily modified to accommodate future integration requirements and potential design changes.

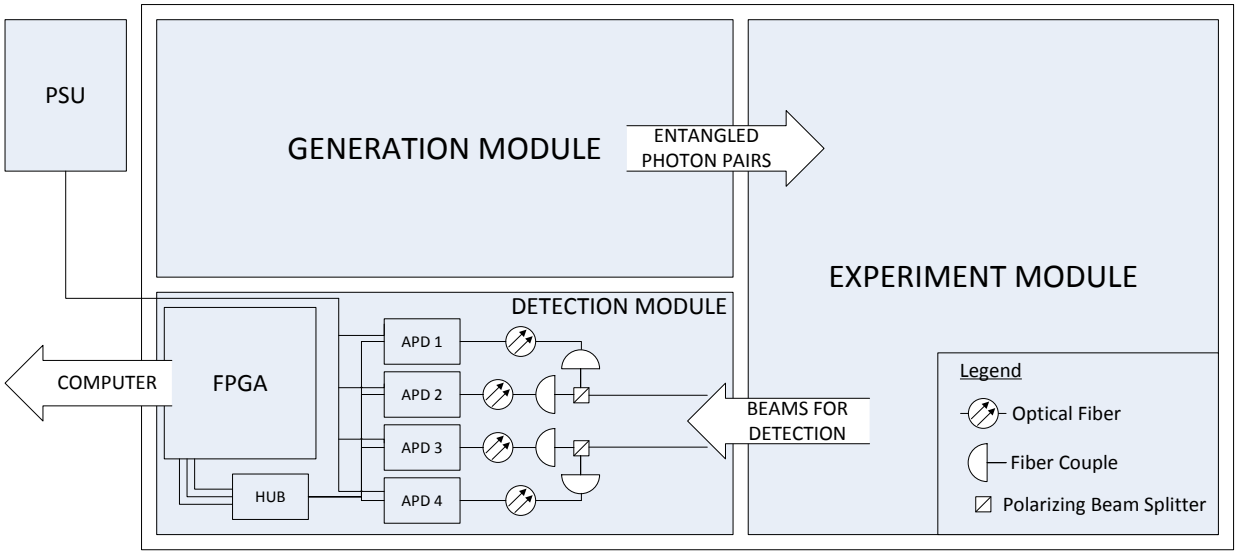


Figure 3: Optical Bench Design

Power Supply

Each of the APDs is powered by a customized desktop computer power supply seen in Figure 4. The power specifications for the APDs are given in the datasheet located in the *List of Documents*. A stock 350 W generic brand power supply is modified to allow connection to the +5 V DC lines using standard banana plugs. Additionally, over-current protection for each APD is incorporated by installing 1.5 A fuses between the main power supply unit and each output line. The fuse ensures that if the current draw were to exceed the rated current of the APD then the power connection will be terminated. For protocols on changing blown fuses see the walkthrough document. The circuit diagram for

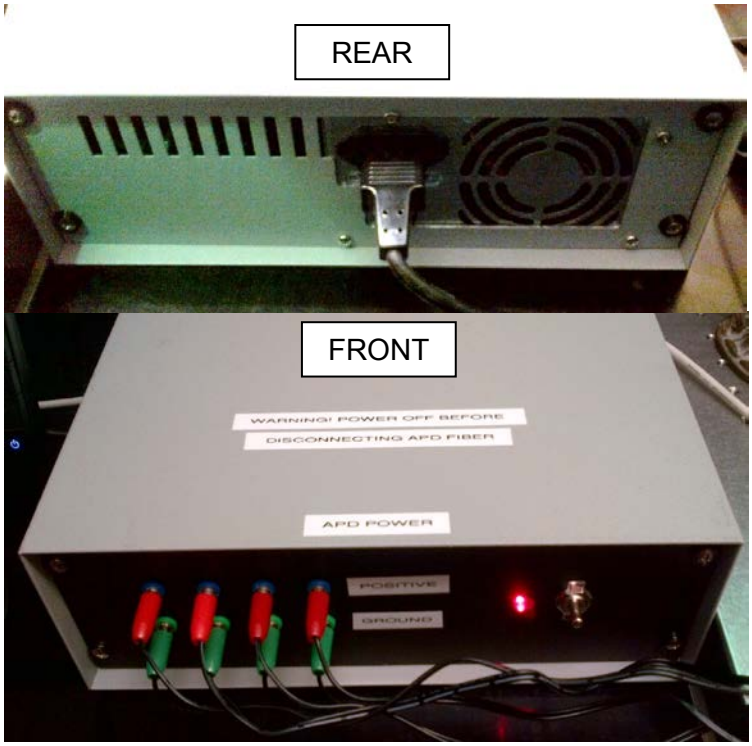


Figure 4: Modified Computer PSU

modifications to the stock PSU is given in Figure 5. Also, high-visibility labels and an LED are placed on the PSU to serve as warnings to students to not detach the fiber optic while powered on.

Low intensity green room lighting was planned to be used to reduce over saturation of the APDs while providing illumination for the room. However, it was found that a significant amount of the light was entering the APDs and causing an increase in detection counts. Therefore, it was decided that best results are achieved when no lights were used while the apparatus was collecting data.

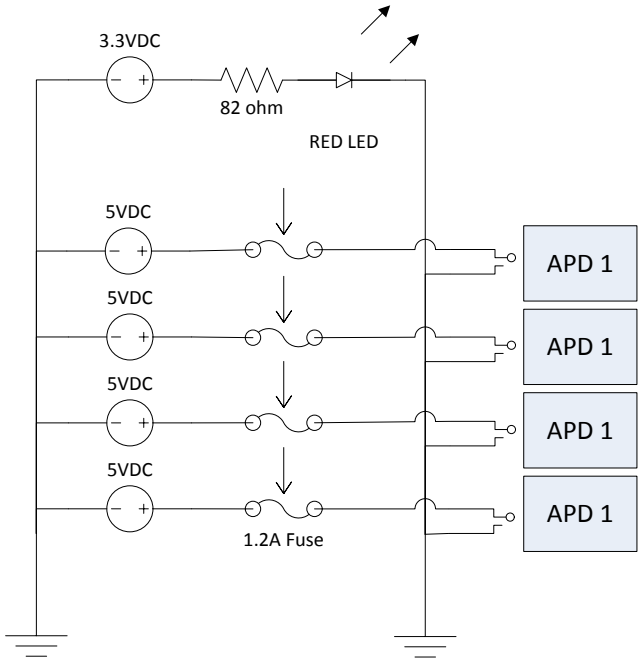


Figure 5: Circuit Diagram for PSU Modifications

The PSU along with all electronics that required a 120 V AC power supply, such as the computer and DE2-115, have been plugged into a wall outlet through a universal power supply (UPS). The UPS provides surge protection for electronics from the main electrical outlet as well as backup battery power in the event of a power outage to protect the computer hard drive as well as the DE2-115 from corruption due to improper sudden power down.

DE2-115 Circuit Housing

The DE2-115 board is mounted on an electrostatic shock resistant material and fastened to the optical table. The main circuit board is encased within a protective clear plastic cover to protect students from electrical shock if touched while powered on and to protect sensitive circuit components from electrostatic damage. Additionally, the DE2-115 on-board switches are made accessible by the student to control signal pulse widths and coincidence windows.

APD to DE2-115 Interface

The digital output TTL signals from the SPCM-EDU CD3375 APDs over BNC cables are communicated to the 40-pin expansion header of the DE2-115 through a custom built hub seen in Figure 6. The 2.2 V output logic of the APDs is found to be sufficient to trigger the 3.3 V logic inputs of the DE2-115 [5]. Figure 7 represents the circuit that was built to convert the BNC outputs from the APDs to a parallel cable input to the DE2-115 using 50 Ω termination resistors. The full enclosure prevents tampering with internal components to improve reliability.

Figure 6: BNC to Parallel HUB

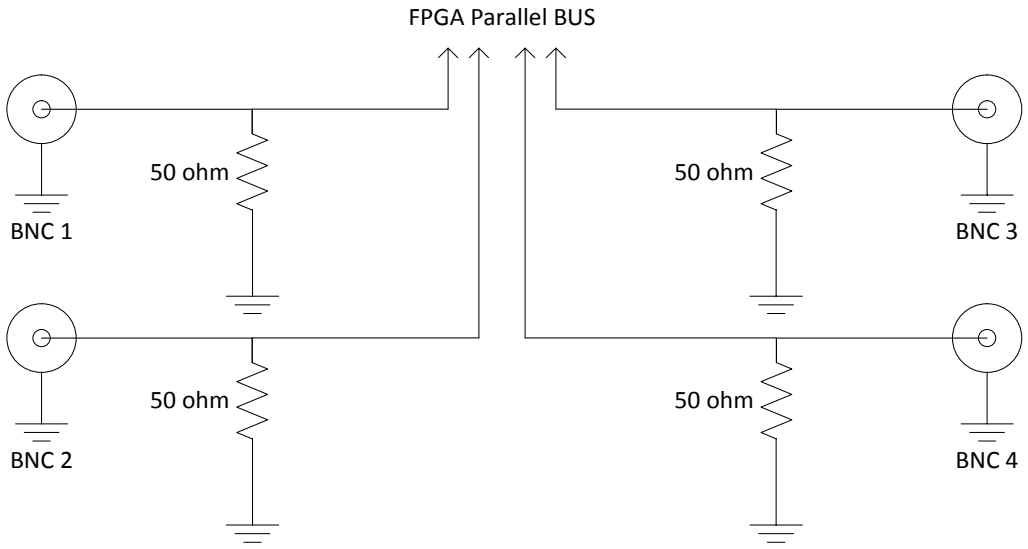


Figure 7: APD BNC to Parallel HUB Circuit Design

Avalanche Photo Diodes

Figure 8: Excelitas APDs

Four identical Excelitas SPCM-EDU CD3375H22332 APDs are used for performing single photon detection (Figure 8). The datasheet, with comprehensive specifications, may be found in the *List of Documents* section of this report. The power cable should be connected to the power input and detection signals are produced on the BNC "output" port. Upon detection of a photon, the TTL output of the APD was measured to be an 18 ns Full-Width Half-Maximum (FWHM), 4.8 V peak pulse. A high speed oscilloscope was used to view this pulse, and the output is shown in Figure 9. Note that upon entering the FPGA, the pulse is slightly distorted and its FWHM shortens to around 14.5 ns. The data sheet also indicates that 35 ns of dead time follow each detection event. Thermal effects cause the photo diode to record false positives called "dark counts" when no light is incident on the detector. Dark counts were measured to be ~400 per second. Also, it was found that the rubber blackout cap used to cover the fiber optic input performed exceptionally well to block light from entering the detectors even when overhead room lights were on.

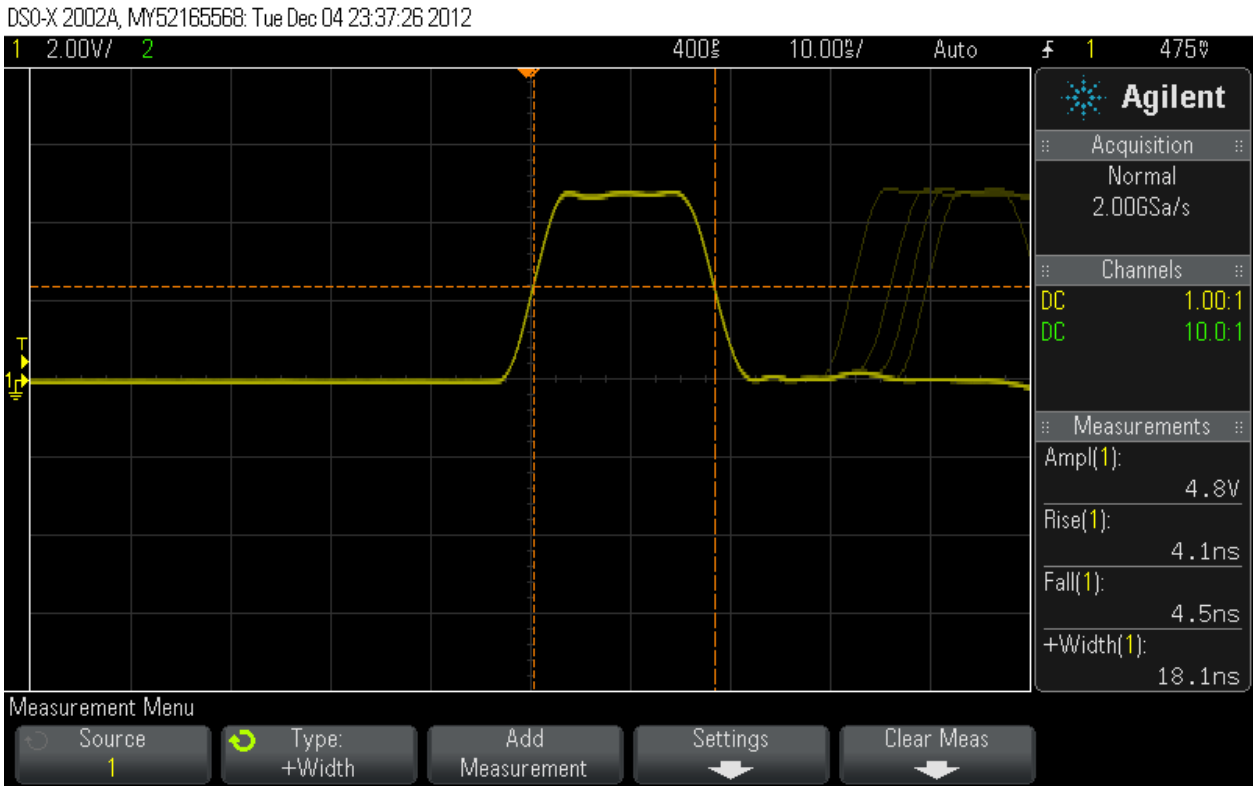


Figure 9: Pulse output from APDs upon detection of photon. Note that upon entering the FPGA, the pulse is slightly distorted and its FWHM decreases to approximately 14.5 ns.

3.2 Circuit and FPGA Logic Design

The final implementation of the coincidence counting logic along with all signal analysis and control is fully contained on the Cyclone IV FPGA of the DE2-115 Development Board. The logic design has been edited from the logic used by both Whitman College [5] and the University of California, Berkeley [6]. The code to program the logic onto the FPGA was written in VHDL and consists of 7 total design files. For more information regarding how the code works, and how to use Quartus to edit the code, refer to the "DE2-115/FPGA README.docx". The code itself can be accessed in the "DE2-115 Project Files" folder on the desktop of the lab computer in MP244. The following sections will provide an overview of the final logic design. A reference schematic of this design is also included in Appendix 9.1 for visual aid.

Pulse Processing

Before the pulses from the APDs can be used to determine coincidences, they must first be shortened from their original length in order to create a specific timing window used for coincidence determination. Due to the method of coincidence detection, the coincidence window directly corresponds to the width of the pulses in time. Hence, to control the timing window, the original pulses from the APDs are first shortened to a desired width. This is performed by ANDing a delayed but inverted version of the original pulse with the original pulse to create a shortened pulse with width equivalent to the delay used. Refer to Figure 10 for a timing diagram highlighting the process.

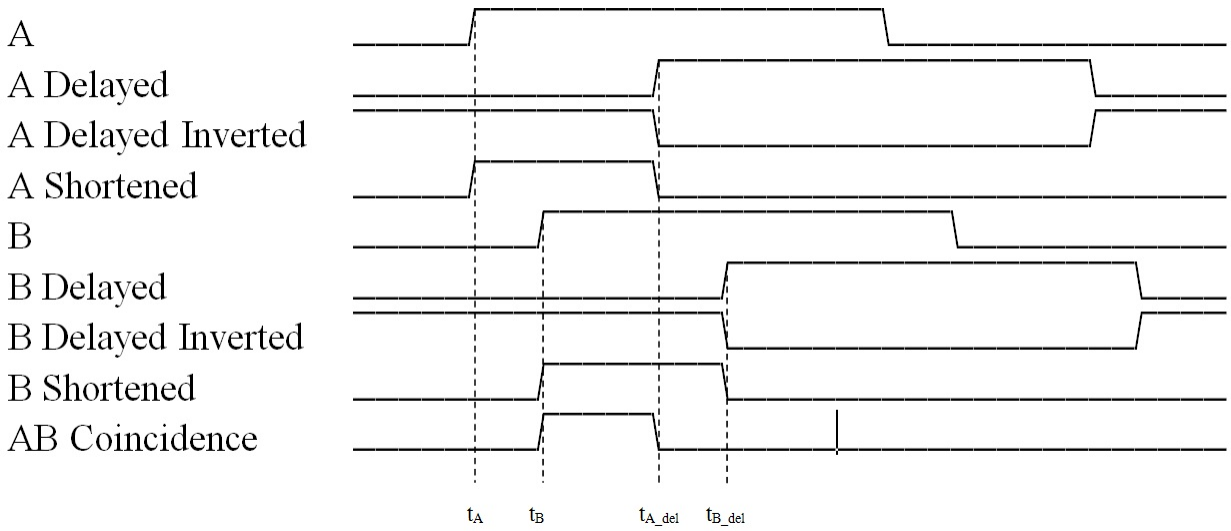


Figure 10: Timing diagram of both the pulse shortening mechanism and the coincidence detection mechanism.

To conduct this shortening in logic, after entering the FPGA the original pulses from each APD are routed through a chain of empty logic cells called LCELLs. Each LCELL adds approximately 0.5 ns to the propagation time of the pulse, but this value differs widely with the physical location of the LCELL on the FPGA, and the FPGA operating temperature and voltage. There are 33 LCELLs used in total, of which only the 31 longest delays are used. To select which delay to use, the delayed signals along with the original pulse are sent through a 32 to 1 multiplexer which uses switches 17 through 13 on the DE2-115 as selectors. In addition to selecting the proper delay, the multiplexer also implements the shortening by inverting the delayed signal and ANDing it with the original.

The particular number of 31 delays was chosen as it allows a continuum of pulse widths to be selected between slightly less than the original pulse width and the minimum measurable pulse width (~2-3 ns) while at the same time minimizing the size of the multiplexer. Rough measurements of all 31 shortened pulse widths have been performed using a high speed oscilloscope and are included Appendix 9.2 along with their associated switch values.

Coincidence Detection

Once the coincidence timing window has been created through the shortening of each pulse, the coincidences between detectors can then be determined. The FPGA contains logic capable of determining all 11 different types of coincidences possible for 4 detectors including two-fold, three-fold and four-fold coincidences. To perform this coincidence detection, the shortened pulses for the coincidence in question are simply ANDed together, producing an output only if the pulses overlap in time. This overlap only occurs if one pulse (say pulse B) arrives after another pulse (pulse A) within the width of the first pulse (pulse A). Hence, as discussed before, the coincidence window is directly proportional to width of the pulses. In fact, due to the independence of which pulse arrives first, the true coincidence window is exactly two

times the width of the pulses. Refer to the bottom of Figure 10 for a simple demonstration of this coincidence determination.

Coincidence Storage

Once the coincidences have been determined, this information needs to be temporarily stored on the FPGA before it can be transferred to the computer for final processing. This is also true for the single counts of each channel as well, creating a total of 15 different quantities which require temporary storage. 15 32-bit counters are used for this purpose, and are incremented by the coincidence signal for coincidence counters or the original pulse signal for single count counters. The counters also possess a reset, which will reset every 0.1 s once a data read-out to computer has been initiated. 32-bit widths are more than sufficient to handle the maximum possible count rate seen by the APDs without overflowing.

Communication Protocol

Finally, the coincidence and singles count information must be periodically transferred to the computer for final processing. To perform this, a finite state machine has been implemented allowing a read-out of all 15 counters every 0.1 s through the DE2-115's RS232 serial connection. To properly time the RS232 connection, a 19.2 kHz Baud clock is implemented which generates a tick every 2604 DE2-115 50 MHz clock cycles. To trigger a data read-out, another counter is used which creates a tick every 1920 Baud clock cycles, or every 0.1 s.

The data trigger first saves the values of the coincidence and single counts counters into latches and then resets the counters such that they can continue storing data during the read-out. The RS232 finite state machine is then activated which successively outputs each bit of the latches over the serial connection. Each RS232 transmission packet uses 1 start bit, 7 data bits, 1 parity bit, and 1 stop bit. It then takes 50 Baud cycles to output one latch, and thus 550 Baud cycles or 32.06 ms to output all 15 latches.

Additional Functionality

The components listed above form the core of the functions for the coincidence counting. Additional features are implemented on the DE2-115 to increase the user friendliness and functionality. Such as, the red LEDs and switches of the DE2-115 are connected to each other allowing the LEDs to easily indicate which switches are turned on, even in low light conditions. Switches 17 through 13 are used to control the coincidence window as indicated in Appendix 9.2. Multiple internal signals are also output on the 40-pin cable for the purposes of debugging. Refer to the DE2-115/FPGA README.doc for a pin-out diagram displaying these signals and their associated pins.

3.3 LabVIEW and GUI Design

Data Processing

As discussed previously, the FPGA communicates with the LabVIEW program through an RS232 serial connection where the program receives a bit-stream every 0.1 s consisting of the 15 coincidence and singles count information. Before this information can be displayed or used for any experiments, LabVIEW must first convert it into a readable format. In order to

accomplish this task, the incoming data stream must undergo several steps within the LabVIEW software outlined in Figure 11.

The first step involves converting the bit-stream into data that can be managed by LabVIEW. The incoming bit-stream from the FPGA is decoded based on the RS232 protocol and is formatted into a sequence of numbers. A loop then breaks down this sequence into an array that corresponds to the read-out from each of the 15 registers. The program can be set to acquire data and refresh over multiple 0.1 s intervals, resulting in an array of the cumulative counts from the registers for that one extended update interval. This large array is then broken down into 15 independent parts that are ready to be displayed.

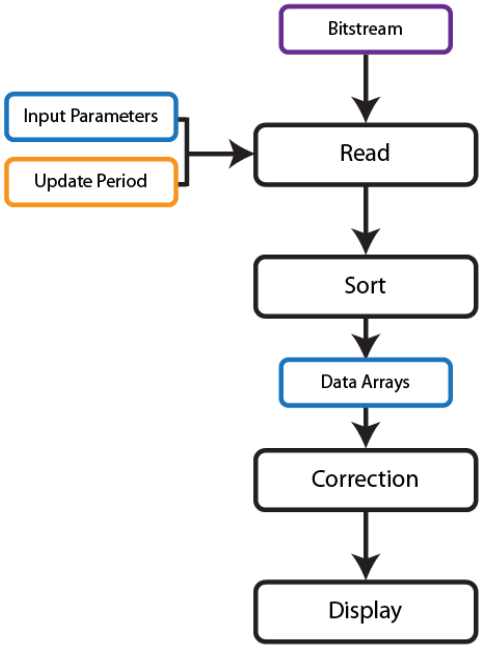


Figure 11: LabVIEW Processing

In order to obtain accurate experimental results, the coincidence information must be corrected for statistical "accidental coincidences". This correction is made by assuming a random distribution of classical photon arrivals within the acquisition time window. This statistical correction is calculated through

$$C_S = \frac{2N_1N_2\tau}{T} \qquad (1)$$

where N_1 and N_2 are the counts read in each channel per update period T, and τ is the timing window. This formula can also be extended to correct for three-fold and four-fold coincidences by multiplying it again by the number of counts in the third or fourth channels. Once this statistical correction is calculated, it is subtracted from the raw counts received by the FPGA, giving a final actual coincidence count. The raw counts, statistical counts, and corrected counts are all displayed on the LabVIEW interface.

LabVIEW Interface

The LabVIEW interface, as shown in Figure 12, displays the single and coincident count data along with a warning light and plot for performing calibrations of the timing window. The features in the figure refer to the following functionalities:

1. RUN button (press only when the FPGA is on)
2. STOP button (stop before turning FPGA off)
3. Input settings: hardware port (COM1 for RS232), total update period, and coincidence window divided by 2 (ie. pulse width)
4. Single photon counts from each detector
5. Coincidence counts: corrected coincidences, statistical correction, and raw coincidences

6. Warning light for “APD Light Level”. Warning light turns red when any of the single count meters saturates, indicating that an unsafe amount of light is picked up by the APD’s (over 1,000,000 photons/s).
7. Graph for determining actual coincidence window. This graph plots the statistical correction against raw coincidences for A-B coincidences. If the light incident on the detectors is classical, and the timing window entered in the interface is the actual timing window, then the graph should plot a straight line, indicating the coincidences are equal to the statistically predicted coincidences.

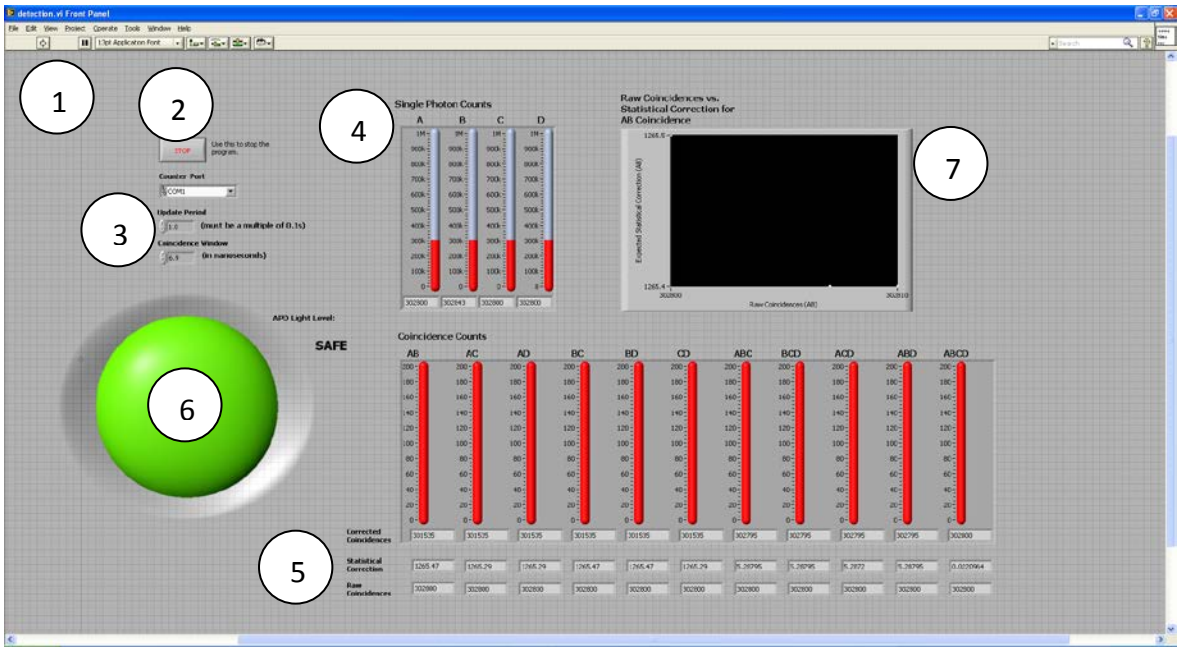


Figure 12: LabVIEW GUI

The interface requires three input parameters from the user: counter port, update period, and coincidence window. The counter port specifies which hardware component is in communication with the LabVIEW software which in this case is the RS232 serial connection. The update period is how often the displayed data is refreshed on the interface, and is selected as increments of 0.1. 0.1 s is the smallest update period due to the read-out rate of the FPGA. Photon counts are shown on the LabVIEW interface for all single counts (corresponding to APDs A, B, C and D) and coincidence counts occurring within the specified coincidence window. Coincidences are reported for all possible APD combinations.

When entering the coincidence window, one must be aware that the value they enter may not be the true coincidence window seen by the FPGA. The coincidence window entered into the LabVIEW interface should correspond to the actual pulse width used in the FPGA. However, the values given in Appendix 9.2 are only approximate, and are not the actual effective widths seen by the FPGA. In order to properly determine the actual coincidence window, a calibration must be performed using the graph displayed on the interface. Using completely classical light incident on detectors A and B, the AB coincidence rate should be

entirely statistical and thus exactly match the coincidences predicted by Equation 1. Hence while plotting the coincidence rate for classical light against the statistical corrections, if the coincidence window used does correspond to the actual coincidence window, a straight line with slope 1 should appear. If the slope is slightly less than or greater than 1, a calibration of the timing window entered can be performed to bring it to the actual value (simply divide the entered timing window by the slope). If the test is repeated using the calibrated value, the graph should then plot a straight line with slope 1, indicating that the statistical corrections do properly correct for ALL accidental coincidences. For more information, consult the Walkthrough document "Walthrough_Final.docx".

Additional Design Decisions

The following design decisions were made to the front end LabVIEW interface after the preliminary design report. First, the scale on the individual counts reads to a maximum of 1 million counts, while the coincidences read to a maximum of 200. Although the scale can be changed on the fly, this change is to account for the low percentage of entangled photons amongst classical light. Secondly, in order to convey the functionality of the statistical corrections in real time, each coincidence counter meter displays the raw counts, the correction, and the corrected counts. This allows for easier verification that the apparatus is calibrated properly. A large safety light was also included that turns red as soon as any individual count goes higher than 1 million counts per second in order to remind users to keep the light level in a safe range. Finally, in order to actively display the linear relationship between the predicted and effective coincidence windows, and to provide a method for calibrating the coincidence window, an X-Y graph is included that plots the readings from the A-B coincidence meter in real time.

Although all of the functionality of the interface is visible on the front panel, the underlying code is found in the "back end" of the visual interface. Details regarding the back end of the LabVIEW software are included in the LabVIEW_README.doc file.

4 Walkthrough

The walkthrough document provides comprehensive operating protocols for the detection module and well as a series of five experiments used to verify correct functionality. The file "Walthrough_Final.docx" can be found in the desktop folder "Detection" of the lab computer in MP244.

4.1 Outline of Walkthrough

The following is a basic outline of the contents of the walkthrough. For more detailed information please refer to the walkthrough document. Prior to operation please read the warnings in the operation protocol section of the walkthrough document. These warnings serve as a guideline to protect the sensitive APD units from becoming damaged from light saturation and overheating.

Operation Protocols

1) Warnings
2) Turning the Detection Module ON
3) Switching to STANDBY Mode
4) Powering OFF
5) Using the LabVIEW interface
6) Changing the Coincidence Detection Timing Window
7) Replacing PSU Fuses
8) Fiber Coupler Alignment
9) Maximum Loading of APDs and Counting Logic

Experiments

1) Turn on and verify basic functionality
2) Pulse generator and verifying counts
3) Verify coincidences
4) Verify pulse shortening mechanism
5) Verify accidentals correction and measure true coincidence window

4.2 Results

All operating protocols and experiments were tested on December 8th, 2012 in MP244 during a mock lab student scenario conducted by the Capstone course professor and teaching assistant who were unfamiliar with the apparatus. The protocols were written in a step-by-step prescribed fashion and the users were able to follow them without error. At no time during the experiments were the APDs in jeopardy of being damaged which indicated that there were a sufficient number of visual warning cues for the user.

Experiments one through four were basic experiments used during the debugging phase of the design process to verify correct functionality. They made use of a pulse generator capable of producing 30 ns pulses, similar in nature to the pulse generated by the APDs. In Experiment 1, the users learned how to turn on the apparatus, and view counts and coincidences on the LabVIEW program. In Experiment 2, the users utilized the pulse generator to witness changes in pulse frequency and thus singles and coincidence counts, as well as correctly verify that the number of counts displayed is the actual number of counts incident on the detectors. For Experiment 3, the users connected different combinations of identical signals to verify that all 11 different coincidences worked properly and output the correct number of coincidences. Experiment 4 involved using voltage probes to probe the shortened pulses output on the 40 pin cable into the BNC Hub and verify that they indeed shorten as expected when the DE2-115 switches were adjusted.

Experiment 5 was a demonstration of the calibration method discussed previously and was found to be extremely important to the functionality of the apparatus. This experiment allows the user to accurately determine the actual coincidence window based on measurements of random coincidences and comparison to statistical calculations. It is the most accurate method of determining the coincidence window and is very reliable. Since the signal-to-noise of the apparatus depends directly on the size of the coincidence window, future experiments

should use the actual coincidence window measured from the experiment when taking data and calculating results.

Each experiment was successfully executed and the desired results were achieved which demonstrated correct functionality of the detection module.

5 List of Documents

The following is a list of additional documents that are relevant to the design project as well as where they can be located.

Document	Location	Audience	Purpose
Entanglement_PartsInventory.xls	Computer Desktop Folder “Detection”	Developers	Contains an inventory of all purchased and needed components for the experiment.
SPCM-EDU_CustomerSpecification.pdf	Computer Desktop Folder “Detection”	Developers, Technical Staff	Datasheet for the APDs
Proposal_Final.docx Preliminary_Design_Final.docx Presentation_Final.docx	Computer Desktop Folder “Detection”	Developers	Documents outlining the design choices made during the design and development of the detection module.
Walthrough_Final.docx	Computer Desktop Folder “Detection”	Users, Students, Developers, Technical Staff	Detection Module Operating protocols and operational experiments.
DE2-115/ FPGA README.docx	MP244 in a box labeled “documents”, Computer Desktop Folder “DE2-115 Project Files”	Developers, Technical Staff	How to use DE2-115, how to use Quartus to edit code/program FPGA, description of code/logic.
LabVIEW README.docx	MP244 in a box labeled “documents”,	Developers, Technical Staff	How to use LabVIEW software.
DE2-115 Systems Disc	Computer Desktop Folder “DE2-115 Project Files”	Developers, Technical Staff	Information which came with the DE2-115. (not submitted with final document)
Optical Component Manuals	MP244 in a box labeled “documents”	Developers, Technical Staff	Operating manuals and datasheets shipped with received optical componenets

6 Final Budget

Budgetary considerations for the full project include items already provided by the client for the experimental setup as of August 2012 as well as specific purchases made to complete the development of the detection module. The purchased materials came in significantly under budget compared to the original proposal. This was due to using a donated computer power supply for building the APD PSU, salvaging a PC computer from the Advanced Lab for use with this experiment and deferring the purchase of an additional two fiber couplers until development of the experiment module.

Provided Inventory

Item	**$CDN Price (tax included)**
FPGA DE2 Board	$318.00
Optical Breadboard (3' x 6' x 2.4")	$2398.00
Down Conversion Entangled Photon Source	$3989.00
Basic Accessories and Tools	$874.00
Fiber-Coupling to Detectors (2-channel)	$893.00
Alignment Laser	$653.00
Bell's Inequality Experiment	$265.00
	Total 9381.00

Purchased Items

Item	**$CDN Price Estimate**
Avalanche Photo Diode Power Supply	$79.94
UPS Surge Protector	$64.40
BNC to Parallel HUB	$25.54
APD and Wire Table Mounts	$35.00
Green Light Bulb	$2.48
	Total $ 207.36

7 Next Steps

The single photon detection module represents the first step in a series of three potential development projects to fully realize the full quantum entanglement apparatus. It was developed with the expectation that it would be integrated into the full apparatus by future students who develop the photon generation source and experiment modules specified in the preliminary design [2]. To complete the quantum entanglement apparatus, future work must be done to design and build the remaining two modules.

The current design of the detection module has been made to allow maximum extensibility to future applications. It has been designed to allow the user unrestricted access to all tools for controlling and analysing coincidence detections between all combinations of APDs through the LabVIEW interface. However, all of these tools will not necessarily be needed by students for performing specific experiments such as Bell's Inequalities, the Grangier Experiment or Hardy's Experiment. Therefore, future work will be required when developing the experiment module to build a LabVIEW interface to display only the relevant information to the student for the specific experiment being conducted. The versatile LabVIEW interface that has been created in this project may be simply inherited by the new program and the specific relevant information may be called on to be displayed to the user. It has been designed to simplify the work that the proceeding developers must do when integrating the detection module with the full apparatus.

With regards to the LabVIEW software, there are also numerous components that warrant future work. Currently, in the back end LabVIEW code, the correction logic is not included as a separate function called in the main VI file. In order to clean up the code and to make it more modular, the correction logic could be implemented as a separate sub-function. Moreover, the X-Y graph included in the VI currently only plots data for coincidences between channels A and B. It would be useful (perhaps to check for systematic consistency) to implement a similar function to extract data between all of the channels.

8 References

[1] James Bateman, Jeff Nicholls, and Zimu Zhu, “Design Proposal: Single Photon Detector Experiment”, 2012 [cited Dec. 17, 2012]

[2] James Bateman, Jeff Nicholls, and Zimu Zhu, “Preliminary Design: Single Photon Detector Experiment”, 2012 [cited Dec. 17, 2012]

[3] "Laser Safety," Office of Environmental Health and Safety [online], Sept. 2012 [cited Dec. 19, 2012], available from World Wide Web: <http://www.ehs.utoronto.ca/services/laserhome.htm>.

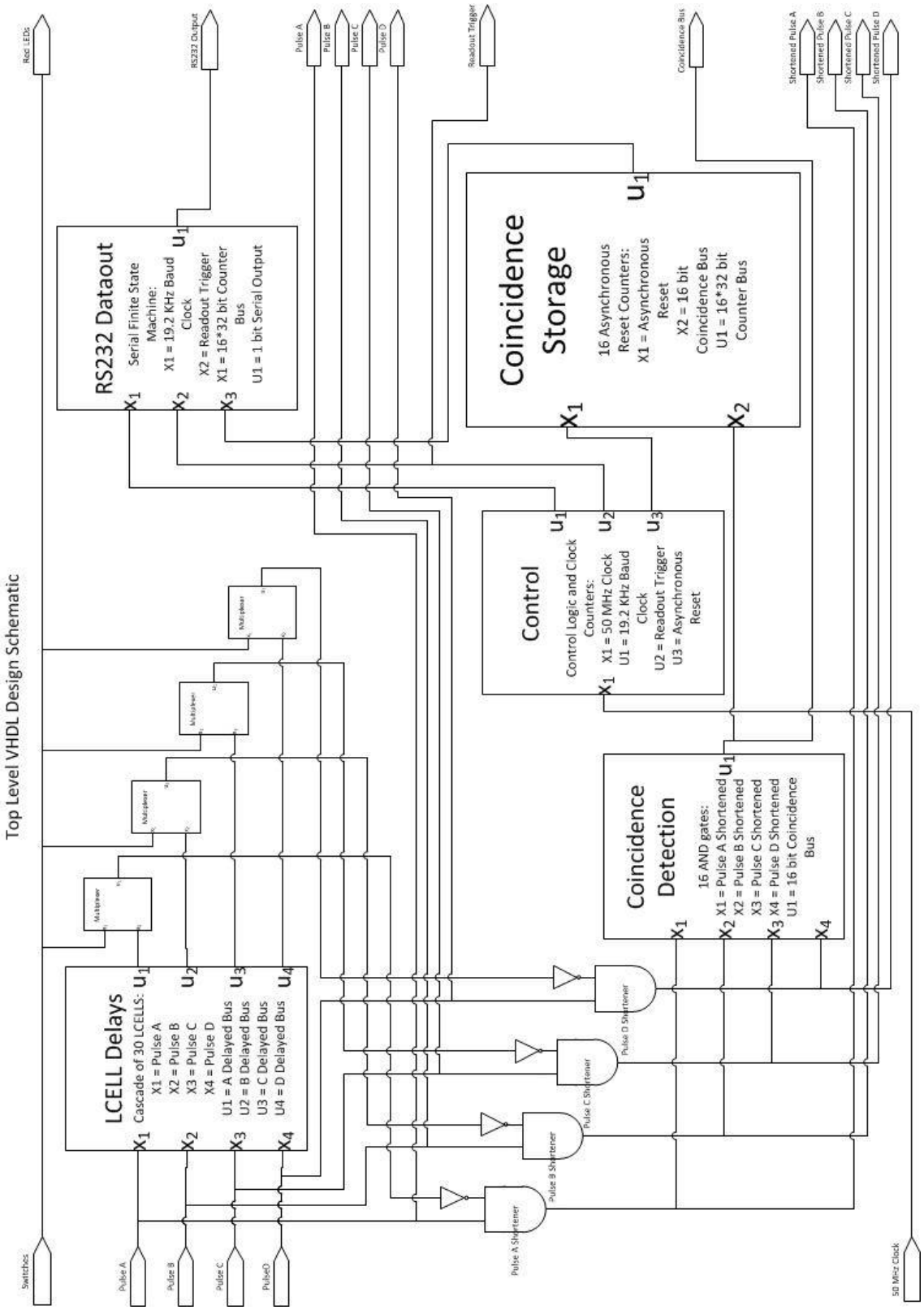
[4] Steinberg Group (personal communication, Oct. 11, 2012)

[5] Whitman College, “Coincidence Counting Units (CCUs)” [online], July 2011 [cited Oct. 19 2012], available from World Wide Web:
<http://people.whitman.edu/~beckmk/QM/circuit/circuit.html>

[6] UC Berkeley Physics Lab,“Design and Documentation (QIE)” [online], Sept. 2012 [cited Oct. 19, 2012], available from World Wide Web:
<http://experimentationlab.berkeley.edu/DesignandDocumentationQIE>

9 Appendix

9.1 Top Level VHDL Design Schematic



9.2 Table of measured shortened pulse widths with switch settings

Estimate of shortened pulse widths with switch selections.		
Switch Setting ("17;16;15;14;13")	**Shortened Pulse Width [ns ± 0.1] (measured @ 2.5 V crossings)**	**Pulse Peak Voltage [V ± 0.05]**
0: "00000"	14.45 (original pulse, no shortening)	5.2
1: "00001"	13.7	5.2
2: "00010"	13.35	5.1
3: "00011"	13.3	5.1
4: "00100"	12.9	5.1
5: "00101"	12.5	5.1
6: "00110"	12.25	5.1
7: "00111"	12.1	5.05
8: "01000"	11.8	5.05
9: "01001"	11.35	5.1
10: "01010"	11.2	5.1
11: "01011"	11.0	5.1
12: "01100"	10.85	5.1
13: "01101"	10.25	5.1
14: "01110"	9.9	5.1
15: "01111"	9.75	5.1
16: "10000"	9.45	5.05
17: "10001"	9.0	5.0
18: "10010"	8.7	4.9
19: "10011"	8.7	4.95
20: "10100"	8.2	4.85
21: "10101"	7.4	4.55
22: "10110"	6.95	4.35
23: "10111"	6.8	4.25
24: "11000"	6.65	4.15
25: "11001"	5.85	3.8
26: "11010"	5.4	3.55
27: "11011"	5.1	3.35
28: "11100"	4.45	3.15
29: "11101"	4.3 @ 2.2 V	2.75
30: "11110"	3.6 @ 2.2 V	2.55
31: "11111"	<2.9 @ 2.2 V	2.4